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Hysteresis in Bio-Organic Field-Effect Transistors

DIPLOMARBEIT

zur Erlangung des akademischen Grades

DIPLOMINGENIEUR

in der Studienrichtung

WIRTSCHAFTSINGENIEURWESEN FÜR TECHNISCHE CHEMIE

Angefertigt am *Linzer Institut für Organische Solarzellen (LIOS)*

Betreuung:

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Linz, Oktober 2006

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Philipp Stadler

Ich möchte mich hiermit sehr herzlich bei Herrn o. Univ. Prof. Dr. Serdar N. Sariciftci, Vorstand des Linzer Institutes für Organische Solarzellen an der Johannes Kepler Universität Linz, für die interessante Themenstellung und die gute Betreuung bedanken.

Mein besonderer Dank gilt Dr. Birendra Singh für seinen persönlichen Einsatz und der Betreuung während der Erstellung dieser Arbeit. Weiters möchte ich mich auch bei allen anderen Mitgliedern des Linzer Institutes für Organische Solarzellen bedanken, die mir immer mit Rat und Tat zur Seite gestanden sind.
Weiters gilt mein Dank den Mitgliedern des Instituts für Physik der weichen Materie für die gute und sehr hilfreiche Kooperation.

Ich möchte mich auch an dieser Stelle bei meinen Studienkollegen für die schöne gemeinsame Zeit während der letzten Jahre an der Universität bedanken.

Herzlich danke ich an dieser Stelle meinen Eltern und all meinen Geschwistern für die große Unterstützung zu jeder Zeit.

Für meine Eltern Hubert und Elisabeth Stadler,
ohne deren Hilfe dieses Studium nicht möglich gewesen wäre.

Hystereseuntersuchungen in Bio-Organischen Feldeffekt-Transistoren

Zusammenfassung

In organischen Feldeffekt-Transistoren kommen verschiedene isolierende Polymere als Dielektrikum in Frage. Ihre dielektrischen Eigenschaften beeinflussen die Transistorleistung, sie sind eine Schlüsselkomponente in der Transistor-Forschung. In dieser Diplomarbeit werden Biopolymere als Transistorkomponente verwendet: Aus Lachs-Abfällen gewonnene Desoxyribonucleinsäure (DNS) wird mit Cetylhexyltrimethylammoniumchlorid modifiziert und als Isolator in so genannten Bio-organischen Feldeffekttransistoren (BiOFET) eingesetzt. Die Resultate zeigen zwei interessante Effekte – zum einen findet sich in der Transistorcharakteristik ein Remanenz-ähnliches Hystereseverhalten wieder, zum anderen ist die Betriebsspannung der Transistoren wesentlich geringer als von organischen Feldeffekt-Transistoren ähnlicher Bauweise mit Standard-Polymeren als Dielektrikum. Die Hysterese-schleifen formen bistabile Zustände, die man für Speicherschaltkreise verwenden kann. Die Wechselwirkungen zwischen dem Dielektrikum und dem Halbleiter an der Grenzfläche zueinander erzeugen verschiedene Raumladungen mit ferroelektrisch-ähnlichen Eigenschaften und werden in diesem Fall für DNS untersucht. Sandwich-Einheiten mit nur Biopolymer (Metall-Isolator-Metall) genauso wie mit Sandwich-Einheiten mit Biopolymer und einer Fulleren – Halbleiterschicht (Metall-Isolator-Halbleiter-Metall) und schließlich Feldeffekt-Transistoren selbst wurden untersucht.

Investigation of Hysteresis in Organic Field Effect Transistors

Abstract

In organic field effect transistors (OFETs) the gate dielectric plays a crucial role - these highly insulating thin film polymer layers are key-components in state of the art organic transistor devices. When replacing the polymer layer by introducing solution-processed thin film modified biopolymer Desoxyribonucleic Acid (DNA) as gate insulator, transistor-characteristics are changed towards remanence-like hystheresis behaviours. The hysteresis-loops probed in bio-organic field effect transistors (BiOFETs) derived from DNA and fullerene derivatives form bistable states which can be used for memory devices at low operating voltage regime compared to similar organic thin film transistors using polymers as gate insulator. Bulk-interface interactions have been reported in various space-charge electrets without ferroelectric-like properties and - in the case of DNA - are probed with sandwich devices of pristine biopolymer (Metal-Insulator-Metal) as well as sandwich devices with biopolymer and semiconducting fullerene derivative (Metal-Insulator-Semiconductor-Metal) and bottom gate – top electrode OFET devices itself.

1. Motivation

When organic polymers with high dielectric constants are used as gate insulators in OFETs, transistor characteristics are changed: Results reported from Singh *et al*. [1] using solution processed polyvinyalcohol (PVA) as gate insulator show hysteresis loops of the source-drain current when it is plotted as a function of the gate voltage (remanent transfer characteristics). These OFETs have bistable states which can be used to store information (memory elements from OFETs, e.g. MemOFETs). Introducing DNA modified with a cationic surfactant as gate insulator, similar remanent behaviour in transistor characteristics is observed with one advantage: The operation voltage is reduced. The reduction of the energy is considered to be one of the key-issues in OFET research. Here promising results in high performance bio-organic field effect transistors (BiOFETs) using modified DNA are demonstrated and motivated us to investigate the function of BiOFETs as well as find an applicable theory for related devices. Apart from low operation voltage the origin of the remanent behaviour is a matter of interest: Considered as an effect from solution-processed lossy bio-organic polymers with slow charge movement in the bulk of the dielectric material, a quasi-permanent polarisation of the dielectric forming bistable states is observed and described qualitatively in this thesis. We note that a simple circuit model here used in this thesis is not sufficient for a full description of a dielectric response of these devices. Further it is shown that the bistability is compatible for the construction of non-volatile low operating voltage bio-organic field effect transistor memory elements.

2. Introduction

2.1. Organic Field Effect Transistor

The basis-function of a field-effect transistor (FET) forms a capacitor, where one plate is a conducting channel between two metallic contacts – the source and drain electrodes - and where the second plate is the gate electrode which can modulate the charge carrier density in the channel by applying a voltage respectively an electric field along the channel perpendicular to the substrate plane. The principle of the field-effect was first proposed by J. E. Lilienfeld in 1930 in a patent [2]. Two decades later the pnp-transistor was introduced by W. Shockley, J. Bardeen and W. Brattain [3] in 1947 and awarded with Nobel Prize in 1955 [4]. The first silicon-based metal-oxide-semiconductor field effect transistor (MOSFET) was fabricated by Kahng and Atalla in 1960 [5]. Working-principles of MOSFETs is based on inversion of the conducting channel and not related to organic field effect transistor working principle. Similar to MOSFET the metal-semiconductor field-effect transistor (MESFET) operates with a Schottky barrier without additional insulating material. In terms of OFET – history one has to mention the thin-film transistor (TFT) as well as the metal-insulator-semiconductor field-effect transistor (MISFET) which both come close to the organic field effect transistor. The first OFET was reported by Koezuka and co-workers in 1986 [6] using polythiophene as semiconductor adopting the architecture of a TFT. State of the art OFETs comprise a flexible large area active matrix display containing 76 800 OFETs [7].

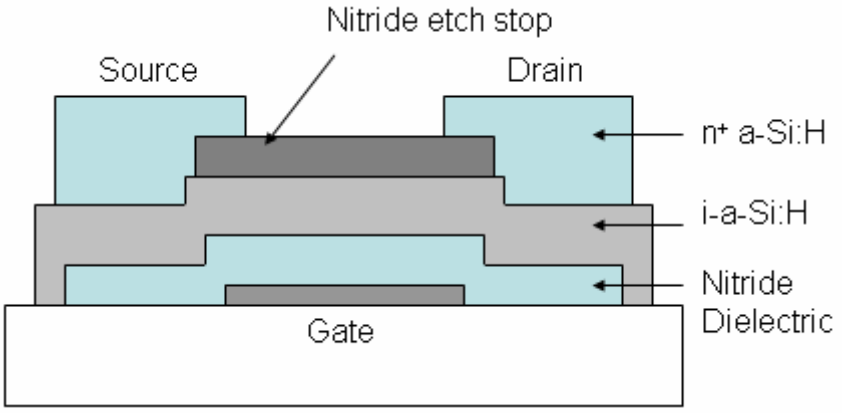

Figure 1 Typical a-Si:H thin film transistor(TFT) structure [8].

In Figure 1 the TFT structure is shown. It has particularly proven its adaptability with low conductivity amorphous hydrogenated silicon (a-Si:H) as semiconductor. One can replace the low conductivity silicon towards organic semiconductors. Many OFETs are based on organic

semiconductor deposited on inorganic oxide layers. Advanced OFET structures use solution-processible polymers as well as small molecule semiconductors. Another materials´ aspect is the gate insulator, instead of metal-oxides results on a broad variety of polymers have been demonstrated [9]. Due to their mutual interface, the combination of organic semiconductors and organic polymer dielectrics shows reasonably good performances in terms of energy consumption and costs-efficiency. Besides dielectric polymers exhibit remanent transfer characteristics too, which is matter of interest for the construction of memory elements [10].

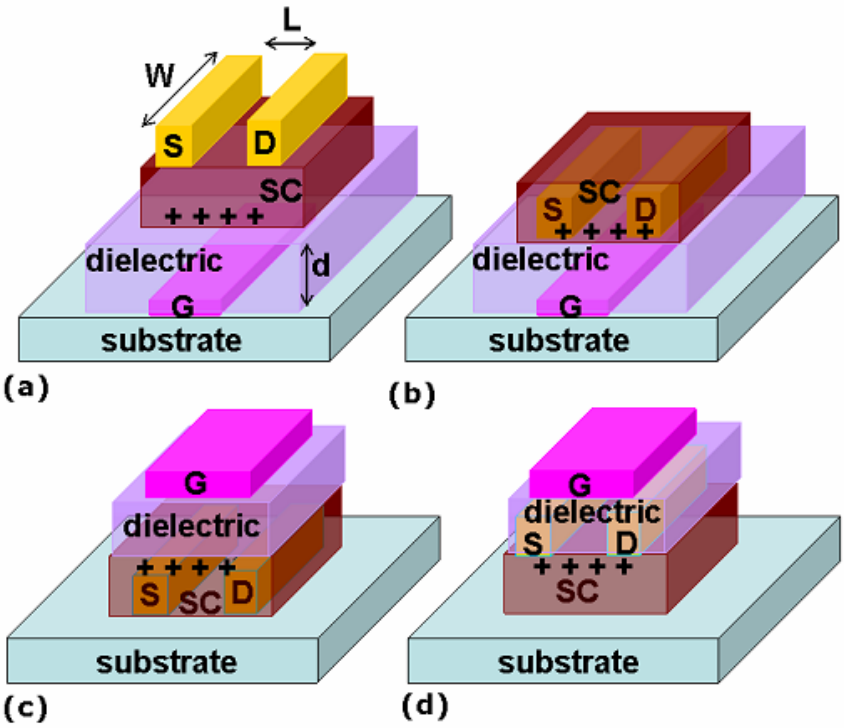

Figure 2 Schematics of p-type semiconductor OFETs with (*a*) bottom-gate top-contact (BG/TC), (*b*) bottom-gate bottom-contact (BG/BC), (*c*) top-gate bottom-contact (TG/BC) and (*d*) top-gate top-contact (TG/TC) structures [11].

Thus, OFETs have been fabricated with various device geometries as depicted in Figure 2. The most commonly realised one is bottom-gate top-contact which again refers to the architecture of thin-film silicon transistor (TFT) using thermally grown SiO_2 insulator on a heavily doped silicon substrate as gate. Promising results using organic dielectrics have been demonstrated recently [12] and the performance of OFETs has improved competetive to amorphous silicon TFTs [11].

2.2. Operating Principle of OFETs

When voltage is applied to the gate electrode the dielectric layer in an OFET is polarised and free charge carriers are induced at the gate dielectric - semiconductor interface: The properties of the active semiconducting organic material layer is changed as seen in a shift of the energy levels in Figure 3. Depending on the work-function of the source metal, the energy level of the organic semiconductor and depending on the polarisation properties of the capacitor-acting dielectric, a certain amount of charges is injected from the source to the semiconductor and a conductive channel arises.

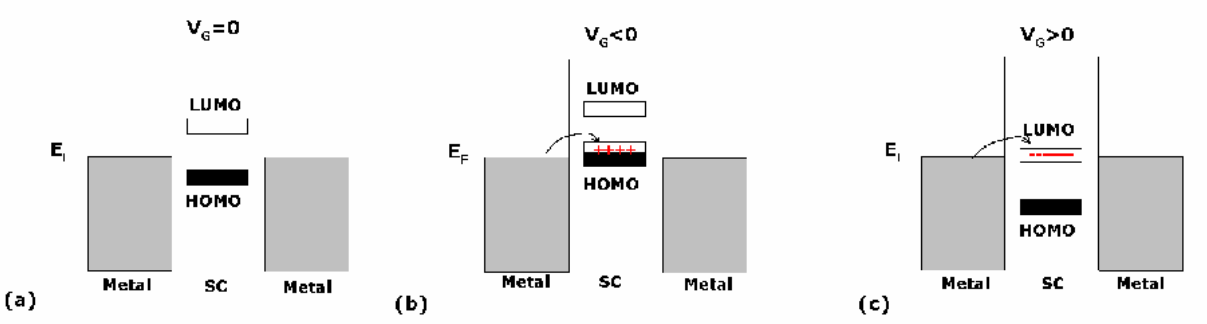

Figure 3 Simplified OFET working principle with respect to applied gate voltage: (*a*) No charges injected when V_g = 0 V, (*b*) injection of holes to HOMO (p-type) and (*c*) injection of electrons to LUMO (n-type) of the organic semiconductor when Fermi level of source/drain metal is close [11].

The resulting charge carrier density in the channel region is a crucial parameter in OFETs, as transport through the channel is heavily affected by the field induced interfacial doping of the organic dielectric and the semiconductor. The gate-voltage driven shift of energy levels allows injection of holes or electrons from the source electrode by accumulating charge carriers in the organic semiconductor (interfacial doping). From Figure 3 one could expect both, injection of holes and electrons to an organic semiconductor. This is only the case for a few ambipolar organic semiconductor materials. A broad variety of organic semiconductors are classified as either n-type or p-type (unipolar semiconductors), determined by their electron-donor or electron-acceptor properties.

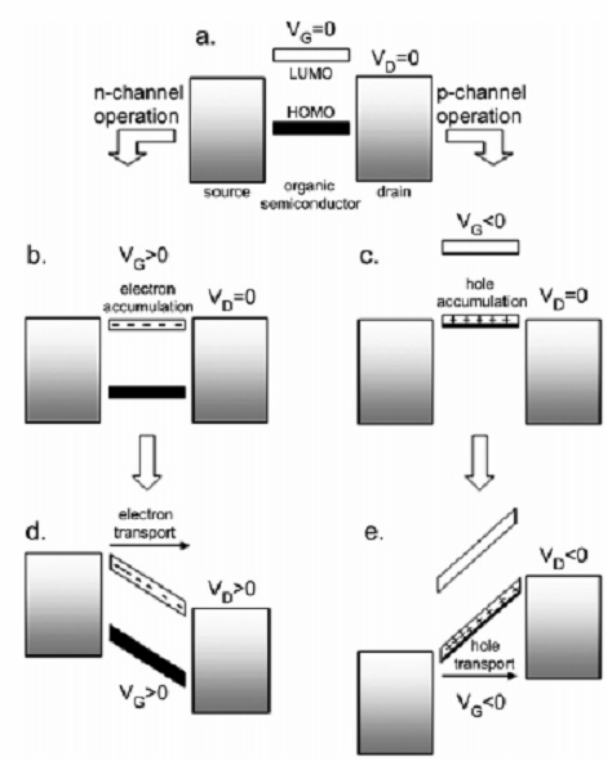

Figure 4 Schematic view of energy-levels in both n-type and p-type organic semiconductors: (*a*) Accumulation of charge carriers from the source by applying positive (*b*) and negative (*c*) voltage to the gate and as a consequence electron- (*d*) and hole-transport (*e*) from source to drain

As depicted in Figure 4 each unipolar class of semiconductor responds to the gate induced field by accumulation of carriers (accumulation voltage), when applying the opposite field a depletion of carriers is observed (depletion voltage). Whenever injection of free charge carriers to the semiconductor takes place the semiconductor is doped. Especially the first few molecular layers at the interface to the dielectric material have a high charge carrier density. A conductive channel arises and current can flow from source to drain presumed that a field is applied across the channel region.

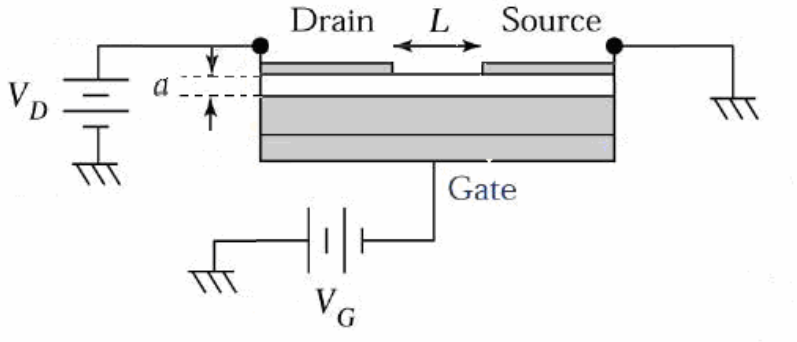

Figure 5 Schematic structure of an OFET when probing characteristics. Both V_g and V_d are grounded with respect to the source electrode.

Figure 5 shows schematically an OFET device using bottom-gate top-contact (BG/TC) structure where the source is grounded and voltage can be applied to the gate (V_g) and to the drain (V_d) with respect to the source electrode (common ground). Important device parameters for current flow are the channel length L, which is the distance between the two metal electrodes and the thickness of the active, semiconducting layer a and the threshold voltage V_{Th}, which describes an activation potential for channel formation. Consequently beside these fixed geometric parameters (channel length and width, layer thickness) and device-specific parameters (threshold voltage, dielectric capacitance) the current from source to drain I_{ds} (transistor current) is a function of the applied field from drain and gate.

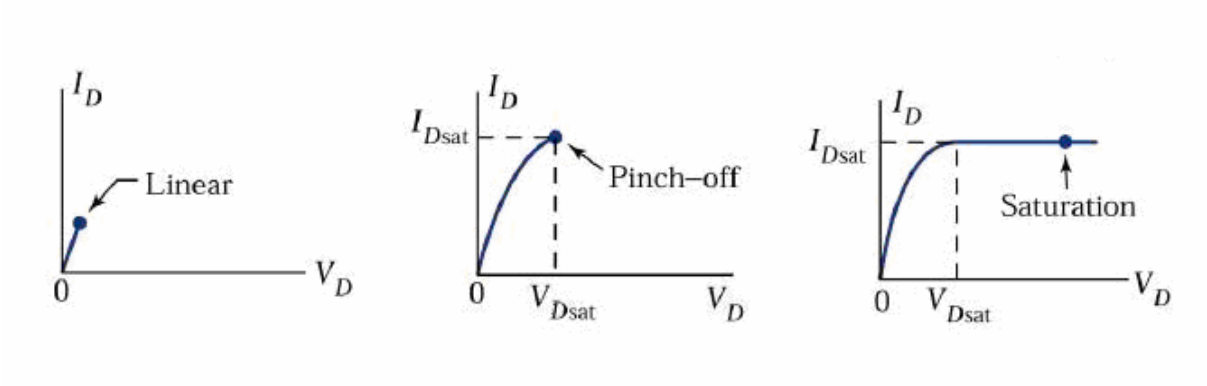

Figure 6 I_{ds} in linear regime, at the pinch-off point and in saturation regime [8].

In Figure 6 three basic V_d operation regimes are illustrated. The gate potential is set to a value bigger than the threshold voltage ($V_g > V_{Th}$). Due to accumulation of carriers a conductive channel is formed which acts like a resistor, when applying a voltage V_d to the drain. Consequently the current I_{ds} is following linearly the increase of the drain voltage. The channel resistance remains constant in this V_d - region. For any given drain voltage, the induced field along the channel increases from zero at the source to the applied field V_d at the drain.

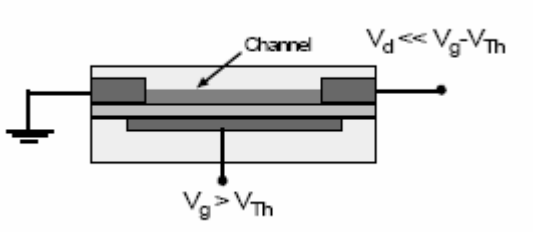

Figure 7 Cross section of OFET device in linear I_{ds} regime. Dark region shows the conductive channel between source and drain electrode.

When V_d is increased further, the depletion layer increases too, and the average cross sectional area for current flow is reduced, compared to the case above. The channel resistance also increases; as a result the current increases at a slower rate, however, there is no longer a linear correlation. When the source-drain voltage is further increased a point is reached where $V_d = V_g - V_{Th}$ at which the channel is "pinched off" ($V_{d,sat}$). A depletion region forms next to the drain because the difference between the local potential and the gate voltage V_g is now below the threshold voltage V_{Th} (Figure 8).

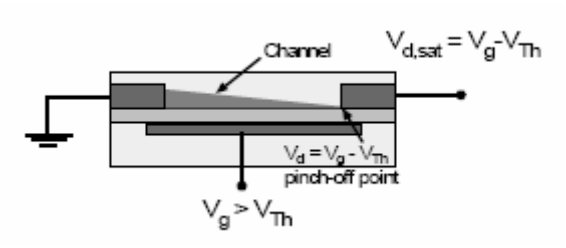

Figure 8 At $V_d = V_g - V_{Th}$ the conductive channel is pinched off by the depletion layer at the drain electrode.

A space charge limited saturation current $I_{d,sat}$ can flow across this narrow depletion zone as carriers are swept from the pinch-off point to the drain by the comparatively high electric field in the depletion region. Since the potential $V_g - V_{Th}$ at the pinch-off region remains constant and thus the potential drop between that point and the source electrode stays the same the current saturates at a level $I_{d,sat}$ as depicted in Figure 9.

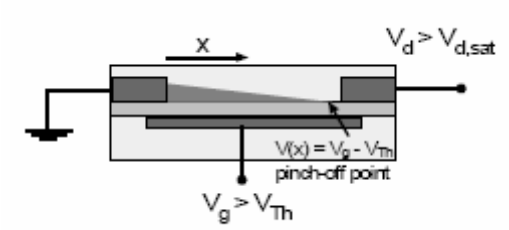

Figure 9 Beyond the pinch-off point $I_{d,sat}$ remains constant. The pinch-off point moves towards the source-electrode.

When a depletion voltage ($V_g < V_{Th}$) is applied to the gate, the initial depletion layer width in the active layer increases and for small V_d the channel again acts as a resistor. Its resistance is higher than above, because the cross sectional area available for current flow is decreased. Vice versa the initial "ground-gate" channel resistance can be lowered by applying a higher accumulation voltage to the gate ($V_g >> V_{Th}$), current flow will increase. Thus, for different gate voltages, output characteristics are shifted to higher currents in case of accumulation and to lower currents in case of depletion.

2.3. Understanding of OFET Device Operation

The saturation behaviour represents one main output of transistor characteristics, there is also the possibility to keep the drain voltage constant, as the source contact is grounded, and the current I_{ds} is measured with respect to the gate voltage (transfer characteristics). Seen in Figure 10, the structure and typical output curves are presented from an organic field-effect transistor with PMMA as gate insulator and PTV as organic semiconductor.

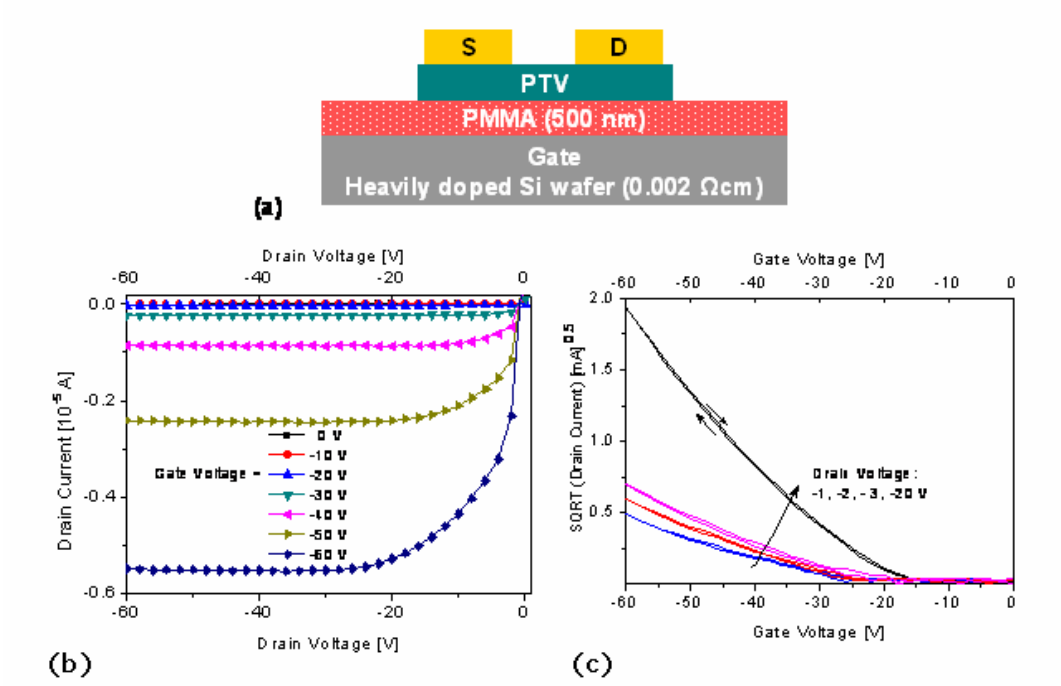

Figure 10 Example of p-type OFET: (*a*) structure of Poly-(3-alkoxy-2,5-thienylene-vinylene) - based OFET with PMMA as gate dielectric, (*b*) output characteristics at various gate voltages and (*c*) transfer characteristics at various drain voltages [11].

In order to describe typical OFET device characteristics device geometry and electrical properties of the incorporated organic materials have to be analysed. Coming back to the basic function of field effect transistor, one of the crucial parameters is the dielectric capacitor where C_p is the geometric capacitance,

$$C_p = \frac{Q_n}{U_{Gate}} \qquad (1)$$

and where U_{Gate} is the voltage applied to the gate electrode and Q_n the number of charges at the interface. Using a parallel plate capacitor with a dielectric (ε_r) the capacitance C_p is defined as:

$$C_p = \varepsilon_0 \cdot \varepsilon_R \cdot \frac{A}{d} \qquad (2)$$

C_p	Geometric capacitance	A	Area of the capacitor plate
ε_0	Permittivity of free space	d	Thickness of the insulator
ε_R	Dielectric constant (relative permittivity of insulator)		

As depicted in equation (1) by applying a field across the insulating dielectric layer, depending on the C_p and thickness of the layer d, energy levels in the semiconductor are bended and it is possible to induce large free carriers from the source electrode to the semiconductor-adjacent to the insulator interface. When energy levels are close to the work function of source/drain-electrode free charge carriers – either holes (p-type) or electrons (n-type) – are injected via the source. The free charge carrier density increases and allows a switch the channel to "on" (accumulation). Main issue is now to find a correlation between the three parameters V_g, V_d and I_{ds}: Starting with the injection of charges from the Fermi-level of the source/drain metal to the energy levels of the semiconductor driven by the field effect from the gate V_g, followed by the field along the channel from source (grounded) to the drain V_d and finally the transistor current I_{ds} flowing through the channel. Besides, an additional effect in OFETs using polymers and organics as insulators are intrinsic interfacial charging effects, along with trapped charge carriers and complex slow dielectric polarisation effects which contribute to charge diffusion in the bulk of the dielectric layer and the interface when an electric field is applied. These effects are summarised as so called complex interface phenomena.

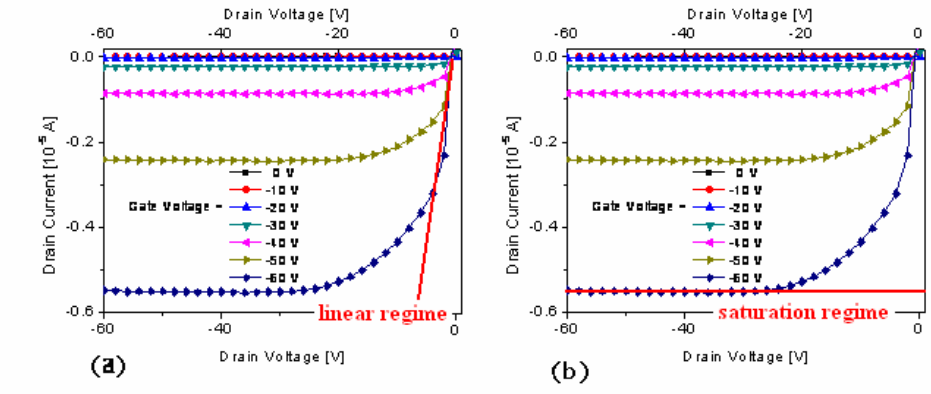

Figure 11 Linear and saturation regime in PTV – OFET [11].

Taking the output characteristics from Figure 10 (*b*), and using geometrical constants as well as capacitance and field effect mobility μ_0 of the semiconductor, the linear increase

demonstrated in Figure 11 (*a*) of I_{ds} at lower drain voltages below the pinch-off point ideally follows this equation:

$$I_{ds} = \frac{W \cdot C_p}{L} \cdot \mu_0 \cdot (V_g - V_{Th}) \cdot V_{ds} \qquad (3)$$

W	Channel width	V_g	Gate voltage
L	Channel length	V_{Th}	Threshold voltage
μ	Field effect mobility [cm² V^{-1} s^{-1}]	V_{ds}	Source-drain voltage

Beyond the pinch-off point current flow becomes independent from the drain voltage and saturates depicted in Figure 11 (*b*).

$$I_{ds} = \frac{\mu_0 \cdot W \cdot C_p}{2 \cdot L} \cdot (V_g - V_{Th})^2 \qquad (4)$$

Constant device parameters for a chosen regime are the W/L ratio as well as in ideal case the geometric capacitance C_p (per unit area of the insulating layer) and to some extend the field effect mobility μ_0. The threshold voltage V_{Th} can be estimated from transfer characteristics when transistor turns on and the current increases exponentially, the term $(V_g - V_{Th})$ represents a normalised value as threshold voltages occur in organic semiconductor devices due to existence of intrinsic charge carriers and work function differences. The current modulation $I_{ds,on}/I_{ds,off}$ as well as the field effect mobility μ_0 are a matter of interest especially in case of high mobilities. In terms of integrated circuits μ_0 gives an idea of the maximum switching frequency f_s of transistor.

$$f_s = \frac{\mu_0}{L^2} \cdot \frac{1}{(V_g - V_{Th})} \qquad (5)$$

The ratio $I_{ds,on}/I_{ds,off}$ is again related to the non-ideal behaviour of OFETs, especially when intrinsic charge carriers allow a low gate independent current flow and leackage currents in the gate insulator I_{gs} will interfere with the off-current $I_{ds,off}$ and determine the minimum current detection limit. Assuming resistances R_p of the insulator in the range of at least GΩ and substantial depletion layer forming, $I_{ds,on}/I_{ds,off}$ -rations of at least 3 to 5 orders of magnitude are reached.

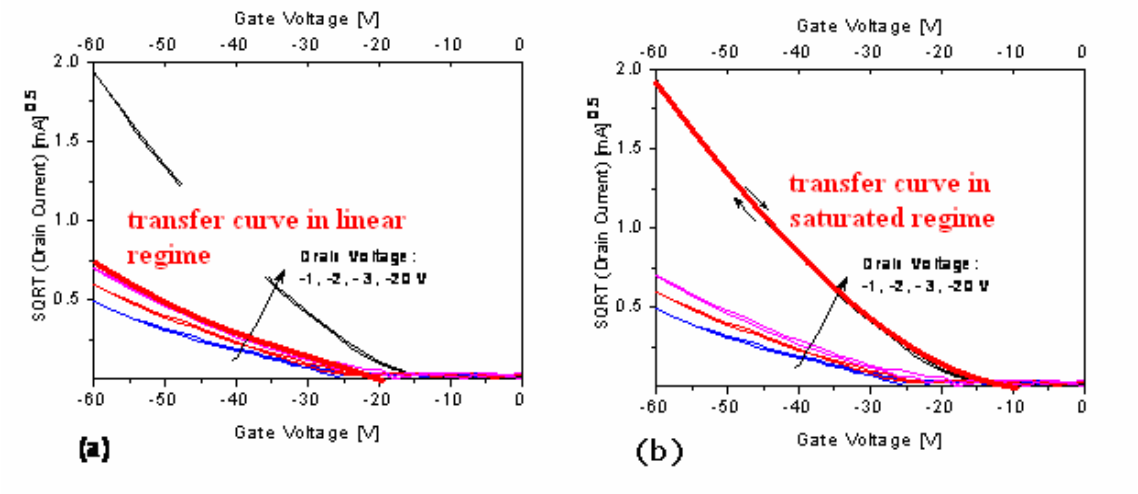

Figure 12 $\sqrt{I_{ds}}$ plotted versus gate voltage. (*a*) red curve is linear V_d – regime and (*b*) red curve is saturated V_d – regime. Square root of I_{ds} increases linearly with applied gate voltage [11].

In order to calculate the field effect mobility μ_0 from transfer characteristics, preconditions should be fulfilled: Using equation (3) the drain voltage is in the linear region and below the pinch-off point respectively. As a function of the applied gate voltage, the square root of the current increases as depicted in Figure 12 (*a*). The slope of the curve is described with the transconductance g_m.

$$|g_m|_{linear} = \left(\frac{\delta I_{ds}}{\delta V_g} \right)_{V_d = cons\tan t} \qquad (6)$$

At low V_d the field along the channel seen by the carriers transported due to the potential difference between the source (grounded) and the drain (V_d) is lower than the field across the field induced by the gate voltage V_g. In this case one can extract the field effect mobility μ_0 assuming that the potential drop parallel to the channel plane is negligibly low compared to the field from the gate perpendicular to the channel plane.

$$|g_m|_{linear} = \frac{W}{L} \cdot \int_0^{V_{ds}} \mu_0 \cdot C_p \cdot dV = \frac{W}{L} \cdot C_p \cdot \mu_0 \cdot V_{ds} \qquad (7)$$

Using equation (3) the linear field effect mobility can be extracted. As shown in Figure 12 (*b*) the calculation of saturation mobility using equation (4) is possible too. When drain voltage is high and beyond the pinch-off point respectively the square root of the current increases linearly with the gate voltage. In saturated regime the transistor current is independent from V_d. When both mobilities are extracted from the same device, values may be different, which is assigned to higher charge carrier density in the saturation regime as compared with low charge carrier density in the linear regime. Theoretical saturation- and transfer-curves can be

described by the listed standard models, which are particularly derived from MISFET – theory. Though the basic principle of MISFETs and OFETs are quite different, organic-based devices emancipate from the silicon-family and form an own branch in terms of both issues semiconductors and dielectrics.

2.4. Lossy Dielectrics, Electrets and Ferro-electrets

One of the interesting issues in OFETs using polymers as gate insulator is the dielectric properties enhanced by the complex polarisation mechanism in dielectric (insulating) polymers [1]. As polymeric layers may exhibit direct current (DC) electrical conductivity, dielectric properties vary with the frequency of the applied field [13]. These so called lossy dielectrics are modelled with a capacitor C_p and a parallel resistor R_p, which refers to a leakage current I_g in thin films shown in Figure 13.

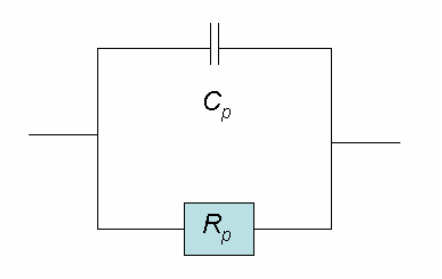

Figure 13 Simplified model of organic dielectric insulator acting as both a capacitor and a restistor

As mentioned in the motivation in chapter 1 using bio-polymers such as modified DNA as gate insulators for fabricating OFETs includes characterising the dielectric properties of the insulating polymer. Summarized in "high-ε dielectrics" with aqueous background, this class of polymers are considered as lossy dielectrics as well as space charge electrets exhibiting a quasi-permanent electrical charge. This consists of real charges such as interface-charge layers and space charges in the bulk of the material as illustrated in Figure 14.

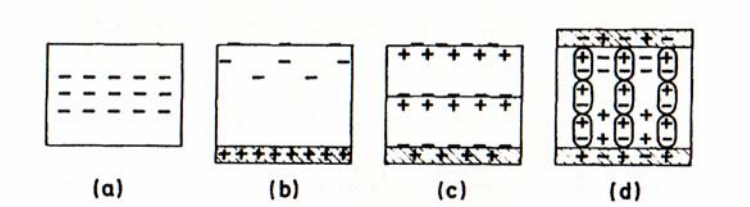

Figure 14 Cross section of space charge electret (*a*) without electrodes (non-metallized monocharge electret). In (*b*) a one-sided metallized electret with surface and space charges and (*c*) with surface charges and charges displaced within domains are depicted. (*d*) shows two-sided metallized electret with dipolar and space charges [14].

Due to the slow polarisation by diffusion of charges in the bulk of the dielectric electret there can be time dependent polarisability of lossy polymeric dielectrics [13]. The fast field effect polarisation is overtaken by slow polarisation effect due to movement of charges in the bulk of the dielectric or in the interface to the electrodes. Furthermore space charge electrets can obtain piezoelectric properties in case of non-centrosymmetrical crystals. Polymers such as Polyvinylidenfluoride (PVDF) exhibit piezoelectricity due to their crystalline regions. In the polar form PVDF is also supposed to occupy ferroelectric-like behaviours because the stable equilibrium crystal polarization can be reoriented with an applied electric field demonstrated in Figure 15.

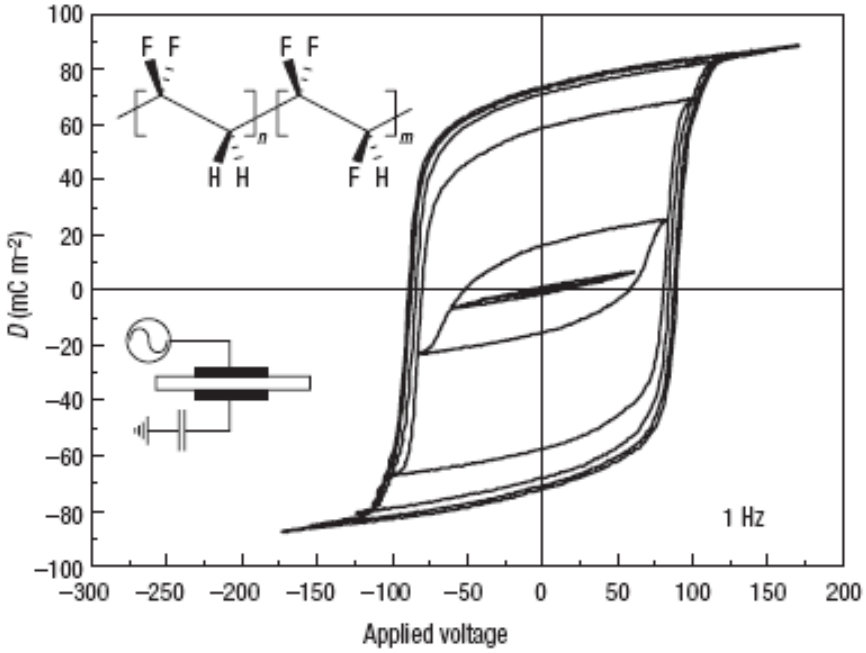

Figure 15 Ferroelectric hysteresis loops of a Poly(vinylidene fluoride/trifluorethylene) copolymer – capacitor device. Thickness of the copolymer-layer is 1.7 μm [15].

A ferroelectric field effect transistor (FeFET) has been demonstrated using remanent properties of ferroelectric-like polymers [15].

2.5. Non-ideal Capacitors

Schematically depicted in Figure 12, if a DC voltage V is placed across a parallel plate capacitor, more charge is stored when a dielectric material is between the plates than if vacuum is between the plates.

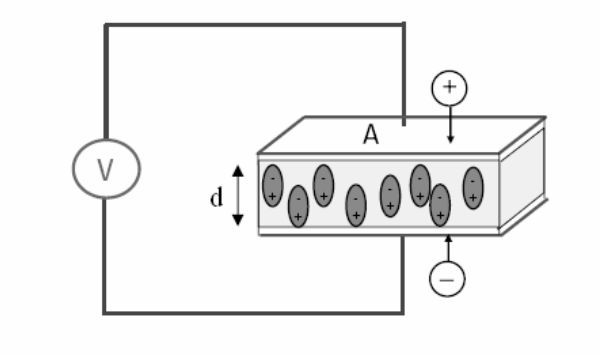

Figure 16 Parallel plate capacitor in DC case [16].

When C_p and C_0 are capacitances with and without dielectric material ε_r is the dielectric constant or permittivity of the dielectric material, ε_0 is the free space permittivity. A and d are the area of the parallel plates and the distances between them.

$$C_p = C_0 \cdot \varepsilon_r \qquad C_0 = \frac{A}{d} \cdot \varepsilon_0 \tag{8}$$

ε_r is a complex term, consisting of a real part ε_r' representing the storage and an imaginary part ε_r'' which represents the loss.

$$C_p = \varepsilon_0 \cdot \varepsilon_r \cdot \frac{A}{d} = (\varepsilon_r' - i\varepsilon_r'') \cdot \varepsilon_0 \cdot \frac{A}{d} \tag{9}$$

When C_p is measured as a function of the frequency f, the dielectric properties are changing at either high frequencies or at low frequencies. An equivalent circle is illustrated in Figure 17, where a non-ideal capacitor is modelled with parallel capacitance and resistance.

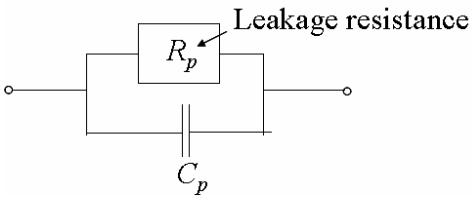

Figure 17 Non-ideal capacitor with C_p and a certain leakage resistance R_p.

Capacitance measurements are based on impedance analysis in AC circuits. The correlation between the impedance X_c and the capacitance of an ideal capacitor is given by the following equation:

$$X_C = \frac{1}{i \cdot \omega \cdot C_p} \tag{10}$$

In order to contribute to losses due to leakage, the impedance Z for a real capacitor is more complex and given by the equations (11):

$$\frac{1}{Z} = \frac{1}{R_p} + \frac{1}{X_C} \qquad Y = \frac{1}{Z} = \frac{1}{R_P} + i \cdot \omega \cdot C_p \qquad (11)$$

The admittance Y is the inverse impedance Z. In equation (12) the real and imaginary part of the capacitance (C_p = C' - iC'') are introduced. In Figure 18 both an ideal and a non-ideal capacitors as a function of the frequency f are illustrated. From equation (11) one expects a straight line for an ideal capacitance. For non-ideal capacitance in high frequency regions the C'' and ε_r'' become relevant and the capacitance changes (see equation 12). More interesting for transistor devices scanning at low frequencies in the mHz regime, changes of C_p are observed too which contribute to ionic diffusion in the bulk of the dielectric (Figure 18). The constricted mobility of ions in an e.g. polymer-electret matrix only allows them to follow field changes in quasi-DC, when scanning at low AC-frequencies. The complex polarisation mechanism of polymer-electrets in low frequency range is considered to be one origin of hysteresis in OFETs.

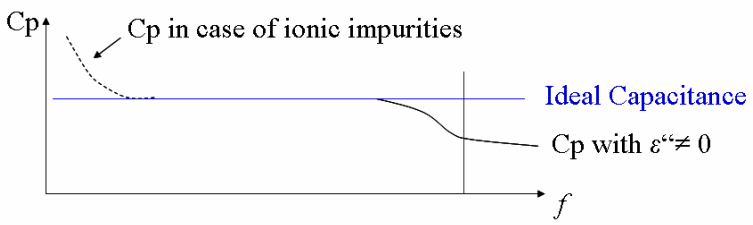

Figure 18 Capacitance spectroscopy: Non-ideal effect at high and low frequency.

Whenever capacitance is measured, the full information of the dielectric has to be provided also in terms of losses. In case of a real, non-ideal dielectric, the capacitance consists of a real part C' and an imaginary part C'' linked to the dielectric constant $\varepsilon_r = (\varepsilon_r' - i\varepsilon_r'')$.

$$Y = \frac{1}{Z} = \frac{1}{R_p} + i \cdot \omega \cdot (C' - iC'') = \underbrace{\frac{1}{R_P} + \omega \cdot C''}_{G} + \underbrace{i \cdot \omega \cdot C'}_{iB} = G + iB \qquad (12)$$

The admittance Y is a complex number with the conductance G as real part and the susceptance iB as imaginary part. The dielectric loss usually is plotted as tangent loss D or $\tan(\delta)$ and mathematically defined as the ratio of the conductance G over the susceptance B.

$$D = \tan(\delta) = \frac{G}{B} = \frac{\frac{1}{R_P} + \omega \cdot C''}{\omega \cdot C'} = \frac{1}{R_p \cdot \omega \cdot C'} + \underbrace{\frac{C''}{C'}}_{\frac{\varepsilon_r''}{\varepsilon_r'}} \qquad (13)$$

The last term (imaginary part of the capacitance C'' over the real part of the capacitance C') describes the ratio of the energy lost per cycle divided by the energy stored per cycle, while the prefactor contributes to frequency dependence ($\omega = 2\pi \cdot f$) and the $R_p C'$ time constant. In case of low resistances R_p or high (or very low) frequencies the prefactor becomes dominant, seen in Figure 19. For an ideal parallel plate capacitor with vacuum in between the loss factor D or tan(δ) is zero.

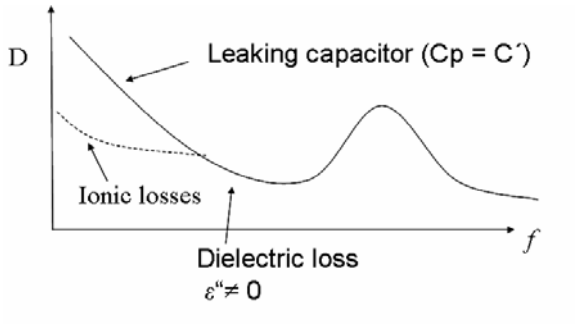

Figure 19 Dielectric losses of a lossy dielectric as function of the frequency

In case of the dielectric capacitor presented in Figure 19 we can describe tan(δ) as a function of the frequency with equation (13) . When analysing a device, normally both values C´ and tan(δ) are shown in order to give a clear picture of the device characteristics. Instead of the capacitance also Z' and Z'' provide the whole information (impedance-spectroscopy). Capacitance spectroscopy is used to detect polarisation processes in various dielectric materials and in case of lossy dielectrics loss effects as well as ionic movement in case of low frequency AC-measurements in the range of mHz (quasi-DC). In terms of transistors metal-insulator-semiconductor metal devices (MIS) are a matter of interest. More complex the double-layer MIS device consists of a metal-insulator, a semiconductor-dielectric- and semiconductor-top-electrode-interface. Here, especially the interfacial doping of the organic semiconductor and the free charge carrier injection process respectively driven by the field-effect can be investigated in these 2-terminal MIS-devices as injection processes go along with capacitance changes.

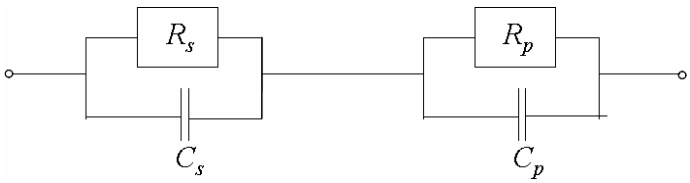

Figure 20 Simplified equivalent circuit to MIS-structure (an additional layer of semiconductor on top of the dielectric layer).

In Figure 20 the circuit equivalent for a MIS device is presented, in series to the insulator (R_p, C_p) an additional parallel capacitor C_s and resistor R_s are added which both contribute to the semiconductor layer. When the capacitance is measured now as a function of the frequency, basically two capacitance-plateaus are expected. These plateaus are demonstrated in Figure 21.

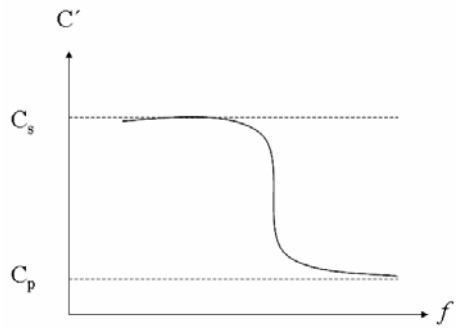

Figure 21 Frequency dependent capactiance in a MIS device, schematically depicted. Expected from both, an plateau for the insulator as well as a plateau for the semiconductor is illustrated.

Scanning from high to low frequency first the dielectric capacitance C_p is seen remaining constant at a certain frequency region. The plateau of the semiconductor C_s arises at lower frequencies which refer to a dielectric relaxation process as an intrinsic property of the semiconductor. Mathematically the capactiance spectroscopy diagram can be approached describing the plateau-building with the Maxwell-Wagner effect:

$$C' = C_s \cdot \frac{1 + \omega^2 \cdot \tau_p \cdot \tau_\Sigma}{1 + \omega^2 \cdot \tau_\Sigma} \qquad (14)$$

The time constants τ_p and τ_Σ refer to the product of the parallel resistance and the capacitance (RC time constant) in the circuit.

$$\tau_p = C_p' \cdot R_p \text{ and} \qquad \tau_\Sigma = C_p' \cdot (R_p \cdot R_s) \qquad (15)$$

Capacitance changes in a MIS device are also observed when a field is applied across the layers. When we choose a sandwich device, with two parallel plates and semiconductor and insulator are embedded in between, and apply a voltage to the electrode on the insulator-side (considered as gate) with respect to the grounded opposite electrode (source), changes in the semiconductor will occur. Carrier injection processes are observed, a simplified schematic overview of the energy levels for a n-type organic semiconductor is presented in Figure 22.

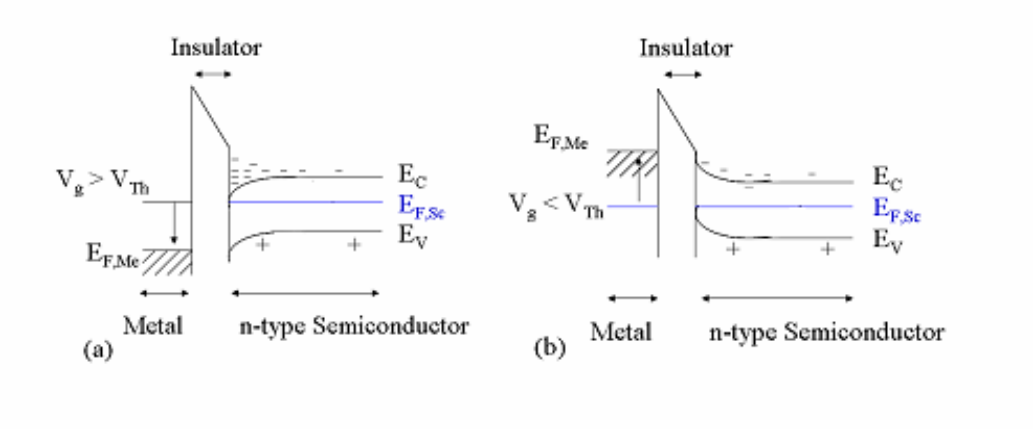

Figure 22 Interfacial doping process of unipolar organic n-type semiconductor: Simplified energy model of Metal-Insulator-Semiconductor device (MIS) in case of (*a*) accumulation and (*b*) depletion.

The double layer device is biased via the gate either to accumulation regime ($V_g > V_{Th}$) or to depletion regime ($V_g < V_{Th}$). E_F represents the Fermi-levels of the metal as well as the semiconductor, defined by Boltzmann-statistics. E_C and E_V characterise the conduction band or lowest unoccupied molecular orbital and the valence band or the highest occupied molecular orbital. When an accumulation voltage is applied to the gate, the insulator is polarised and the conduction band of the semiconductor is bended downwards. Charge carriers (electrons) are now injected from the top electrode (semiconductor-metal interface). As a function of the gate induced field one observes an increase of the capacitance due to an increase of so called free charge carriers. In case of depletion, when the gate is biased with the opposite voltage, bands are bended upwards. In case of an unipolar n-type semiconductors the hole-injection barrier is very high and the amount of free charge carriers cannot be increased by a negative gate bias for hole-transport region. The capacitance observed remains constant. Figure 23 shows a plot of capacitance as a function of the gate voltage as well as the dielectric loss.

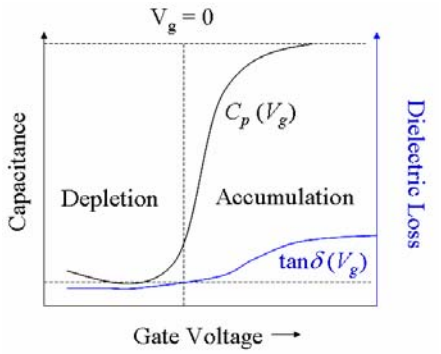

Figure 23 Scheme of Capacitance-Voltage measurement using n-type semiconductor: Black curve describes the increase of capacitance when accumulating carrieres, blue curve relates to dielectric loss in MIS structure.

Capacitance changes observed in transistors are usually neglected when mobilities are calculated, especially in OFETs using equation (4) for the saturated voltage region. The geometric capacitance in equation (4) contributes to the ε_r value of the dielectric layer, the increase of the capacitance in OFETs in accumulation regime contributes to the injection of carriers from the source to the semiconductor. It is to be discussed if calculation of mobilities at saturated drain voltage region especially for high-ε_r dielectric materials is valid.

2.6. Hysteresis in OFETs and non-volatile Memory Elements

Hysteresis loops in bare thin film dielectrics are reported by Naber *et al.* as demonstrated in Figure 15. Question now is, if these dielectric materials are suitable for fabrication of OFET – based memory devices [15]. A non-volatile OFET memory element (MemOFET) have recently been fabricated using OFETs based on organic semiconductors and space charge electrets as gate dielectric by Singh *et al.* [1]. Due to their mutual interfaces trapping effects summarized in complex interface phenomena are seen in transistor characteristics leading to remanent transport characteristics. Compared to the relatively high operating voltage regime in ferroelectric – FETs, OFETs using space charge electrets operate at lower voltage regimes and are applicable for memory elements.

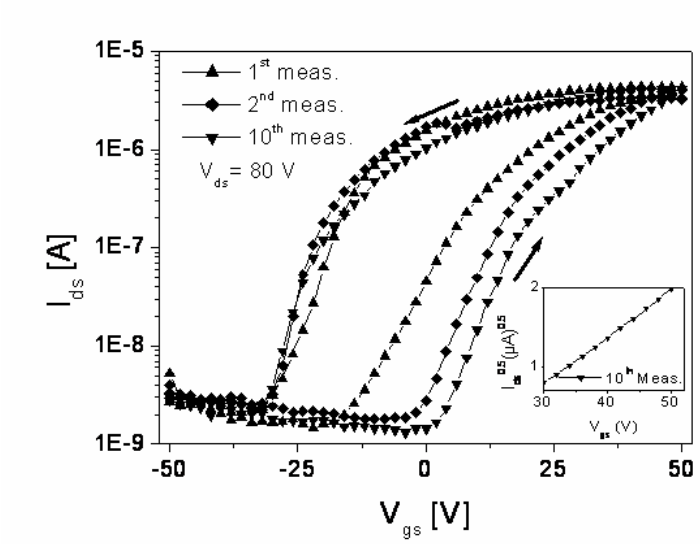

Figure 24 Transfer Characteristics of OFET using Poly(vinylalcohol) as gate insulator: Hysteresis shows bistable state when comparing forward and reverse curve [1].

When a non-volatile MemOFET is characterised, reversing the gate voltage V_g features large metastable hysteresis (see Figure 24) with a long retention time due to quasi-permanent charge storage in the bulk of the gate dielectric or interface of the gate dielectric and the semiconductor. Charge carriers (space charges) inside the insulating layer will move with the field towards the gate and the interface to the semiconductor respectively. This causes additional polarisation due to charge state at the bulk and at the interface. Compared to the fast channel forming from the field effect polarisation, the movement of charges in the bulk of the insulator and consequently additional polarisation and charge carrier injection is considered to be much slower: This resulted in the slower saturation of the current and hence slower decay of the current in OFETs characteristics. Switching the gate induced field

between accumulation, ground and depletion regime within minutes, metastable retention curves can be detected when it is measured as a function of time.

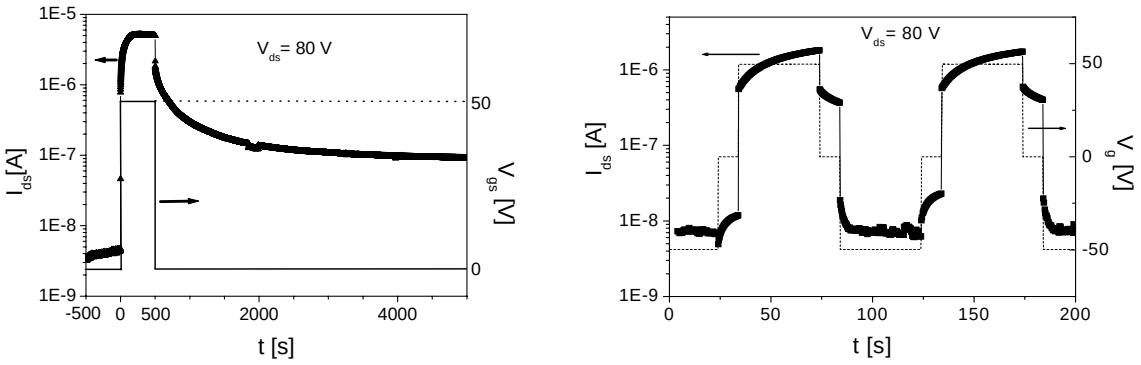

Figure 25 Non-volatile OFET memory element: (*a*) Switching the gate voltage (dashed line) between accumulation, depletion and ground (V_g = 0) and measuring transistor current I_{ds} as a function of time. (*b*) Retention curve: After accumulation pulse current I_{ds} decreases slowly and remains high compared to current level before the accumulation pulse [1].

As depicted in Figure 25 (*a*) the transistor current is low before pulsing the gate into accumulation regime and it remains high after the pulse unless an depletion voltage is applied and decreases the current by several orders of magnitude. In terms of memory element current stages are called “write”, “on”, “erase” and “off” (see Figure 26).

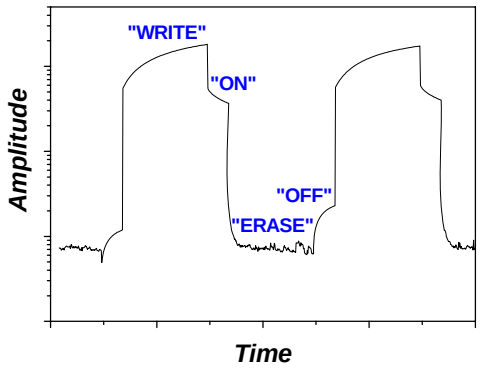

Figure 26 Schematic function-circle of OFET memory device: 4 amplitude-stages complete the circle: “Write” in accumulation mode, “on” in floating (V_g = 0 V) mode, “erase” in case of depletion and “off” again in floating mode.

Referring again to Figure 18 (*b*) the basic question concerns the current viz how stable it will be in the “on” state and how fast it will decrease respectively. From the data above a fast decay at the beginning is followed by slow decay leading nearly to saturation after several minutes. At this level charges are trapped in the interface and charge carrier density remains

high enough to form a conductive channel. Comparing both the channel forming and the deforming process matter of interests are two competing effects: A fast injection of charge carriers due to gate dielectric polarisation on the one side and the slow injection of carriers by charge movement in the dielectric/interface and quasi-permanent states. We can observe these effects (hysteresis and metastable states) when the current is measured as a function of time.

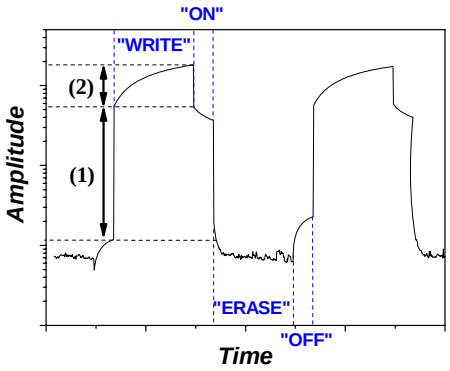

Figure 27 Stages of charge carrier injection: (1) Fast forming of conductive channel due to field effect from accumulation voltage. (2) Slow injetion of charge carriers from charge movement in the insulator and logarithmic increase of current I_{ds} at constant accumulation field from gate.

As illustrated in Figure 27 at constant field current increases further. This slow channel forming observed can be indicative of presence of ionic/slow moving charges. Consequently at lower temperature slow channel forming effects alias slow polarisation effects of the dielectric are disappeared as these charge diffusion is inhibited due to immobilisation in the insulator matrix [12].

3. Experimental

In this section I will introduce and summarise the pioneering work done at Chitose-Research Institute (Tokio, Japan) and Air Force Research laboratory (Dayton, Ohio) bond on extraction and purification of DNA bio-molecule from salmon followed by the whole integration prosess of DNA into transistor devices done on the Linz Institute for Organic Solar Cells (LIOS). Along with the integration process the device characterisation experiments are explained.

3.1. List of Instruments

- 2 Channel (High Power / Medium Power) Source Monitor Unit E5273A (Agilent Technologies)
- 80 MHz Function / Arbitrary Waveform Generator (Agilent Technologies)
- Precision LCR-Meter 20Hz – 1 MHz 4284 A (Hewlett Packard)
- Cryostat – Optistat (Oxford Instruments DNV)
- Intelligent Temperature Controller ITC 503 (Oxford Instruments DNV)
- Alpha-A High Performance Frequency Analyser (Novocontrol)
- High Voltage Booster HVB 1000_156/0 (Novocontrol)
- Digital Multimeter 236 Source Measure Unit (Keithley)
- Glovebox MB 150B-G / MB 200B (MBraun)
- Evaporation Machine UNIVEX350 (Leybold)
- Evaporation Control AS 053 (Leybold)
- Evaporation Control IL820 (Intellemetrics)
- Scanning Probe Microscope NANOSCOPE IIIa Dimension^{TM} 3100 Series (Digital Instruments)
- Spincoater Model P6700 Series (Speciality Coating Systems Inc.)
- Ultrasonic S 10H Elmasonic (Elma)
- Ultrasonic 150S (Sonomatic)
- Stirrer RH Basic 2 (IKA) IKAMAG RH
- 4100 Digital Multimeter / Switch System Integral Series (Keithley)
- Turbo Pump / Vacuum Turbo Cube (Pfeiffer)

3.2. List of Materials

In table 1 there is a list of all chemical substances and metals used for device fabrication.

Table 1 List of all materials

Substance		M / g mol^{-1}	Company & Purity
Aceton	C_3H_6O	58.08	J. C. Baker, p.A.
Isopropanol	C_3H_8O	60.10	J. C. Baker, p.A.
n-Butanol	$C_4H_{10}O$	74.12	J. C. Baker, p.A.
Hellmanex	-	-	Hellma
DNA (chapter 3.3.)	-	300 000	
Chlorbenzene	C_6H_5Cl	112.56	J. C. Baker, p.A.
[6,6]-Phenyl-C_{61}-butric acid Methylester (PCBM)	$C_{72}H_{14}O_2$	910.90	Nano-C
Cetyltrimethylammonium-chloride (CTMA)	$C_{19}H_{42}ClN$	319.30	Sigma Aldrich
Silver Paint	Ag	107.87	Sigma Aldrich
Chromium	Cr	51.99	Oegussa
Gold	Au	196.96	Oegussa
Aluminium	Al	26.98	Oegussa
Lithiumfluoride	LiF	25.94	Sigma Aldrich

3.3. DNA – CTMA as Dielectric Insulator

DNA derived form marine waste products and modified with surfactant demonstrates excellent passive and active optical properties [17]. The suitability in electro-optic waveguide devices has been proofed – optical memory and optical amplifier applications make DNA-CTMA also interesting for electronic usage as insulating layers [18]. The film quality in terms of smothness and ability of self-assembling is a basic requirement in optical research too and the reproducable scientific work on DNA based films is the fundament of the idea using it for electronic insulator applications.

3.3.1. Origin of DNA – CTMA Complex

Based on the work of L. Wang *et al*. [19] it has been demonstrated that DNA is available in large scale for an applicable self-assembled bulk film material. As an anionic polyelectrolyte modification treatment of DNA is done with cationic lipid-like surfactants rendering a highly organised assembly and enhanced mechanical properties. Originally DNA is derived from salmon waste products such as milt and roe sacs [20]. After treatment with enzymes for protein elimination by protease, proteins are removed by controlling the pH level to 7.5. The material undergoes further cleaning steps such as freeze-drying and filtration after active carbon treatment for decolourisation.

Figure 28 Purified, dried salmon DNA dissolution ready for further treatment (blade-shearing, sonification, ion-exchange) [17].

Exhibited in Figure 28, the final product is a DNA dissolution, which is available for a bright assortment of different molecular weights starting from 8 000 kDa down to 200 kDa with a purity of 96%.

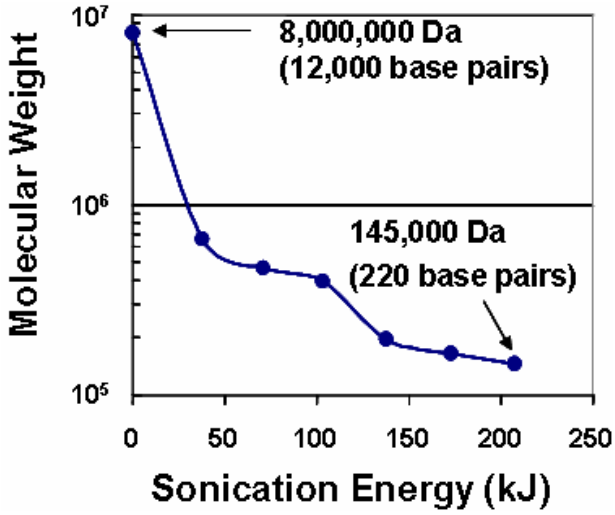

Figure 29 Mechanical modification ot the molecular weigth of DNA. By blade shearing and sonification relatively large batch sizes up to 4 g are obtained [18].

The molecular weight is measured using gel phase electrophoresis. 2 % of proteins still remain in the water-soluble dissolution. For processing the DNA dissolution with lipid surfactant CTMA it is first dissolved in deionised water and stirred for 6 hours. The desired concentration for ion exchange reaction is 6 g l^{-1}. From the CTMA surfactant a solution with the same concentration is made and drop-wisely the same volume added to the DNA solution. The schematic of the ion-exchange reaction is illustrated in Figure 30. It continuous to stir for 6 hours, afterwards the precipitate is separated by filtering using a nylon filter 0.45 µm pore size. The last steps are to rinse the material with deionised water unless the water coming out is clear and bubble-free followed by drying over vacuum for a couple of hours.

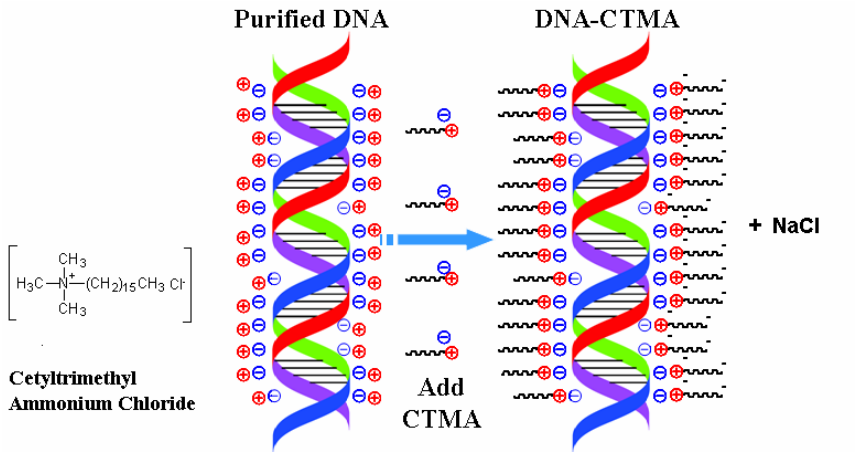

Figure 30 Ion exchange reaction in water of Na-DNA with cationic lipid CTMA surfactant forming a water-insoluble DNA-CTMA complex and sodium-chloride [17].

The dry, white powder can be dissolved in different organic solvents such as n-butanol. It forms a clear homogenous solution; before film fabrication the solution is filtered once again using 0.2 porous filter. Experimentally shown unfiltered solutions of DNA-CTMA complex form comparatively roughter surfaces as the filtered ones. For this reason, 300 kDa molecular weight DNA is preferred for usage in film fabrication as higher molecular weight DNA CTMA solutions are difficult to filtrate.

3.3.2. Properties of DNA-CTMA Complex

Concerning material and surface properties recent results done on use of DNA-CTMA complex as dielectric layer films for OFETs are presented here referring to publications of Singh *et al*. [21] and Wang *et al*. [19]. In general surface roughness and structure of the thin film play a crucial role for use of any insulating dielectric film for OFET. This stems from the fact that the charge transport takes place at the interface of dielectric and semiconductor film.

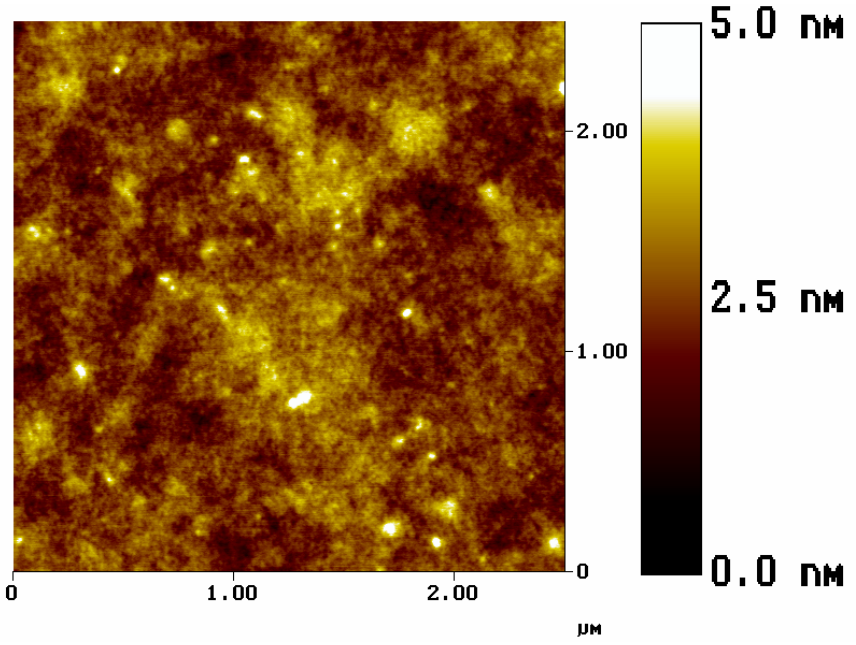

Figure 31 AFM tapping mode image of a 200 nm DNA-CTMA thin film on quartz.

In Figure 31 the surface morphology is presented. The film casted on a quartz substrate shows a smooth surface, with surface roughness of less than 5 nm. The double-helical self-organized structures from pristine DNA are suggested by separated studies [20]. Profound studies on the effect of different chainlengths in the cationic surfactants in DNA-surfactant complexes are presented in the publication of Wang *et al*. [19] including mechanical studies with thermogravimetric analysis (TGA) as well as dynamic mechanical analysis depicted below in Figure 32.

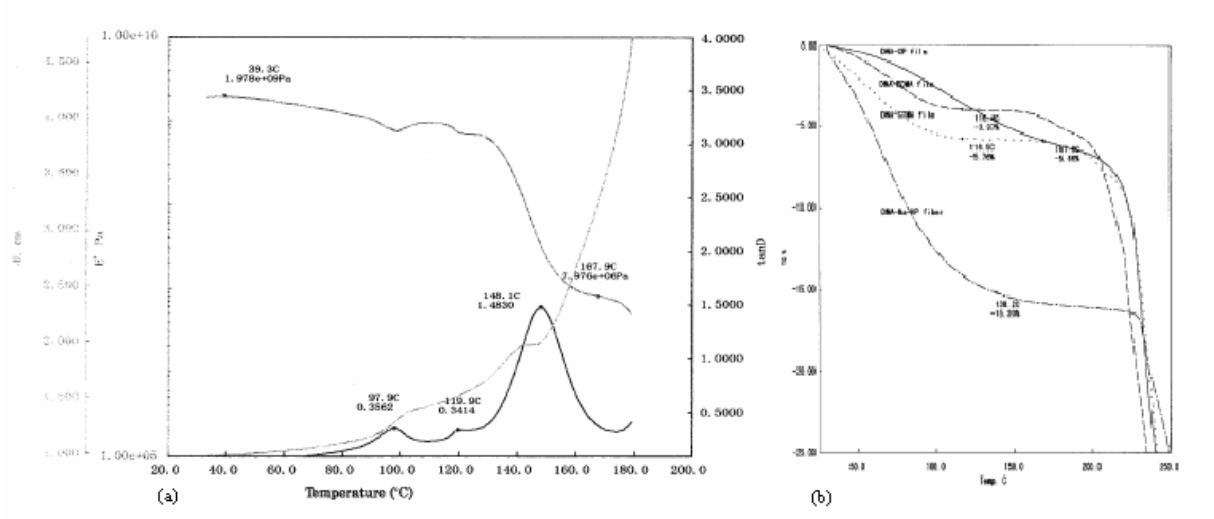

Figure 32 Mechanical Properties of CTMA-DNA films: (*a*) Dynamic mechanical analysis of the DNA-CTMA film at an applied frequency of 1.0 s^{-1} and (*b*) thermogram from films derived from DNA, DNA-CTMA, DNA-BDMA, DNA-CP [19].

Apparently 3 peaks occur in the dynamic mechanical thermogram, the first one around 100 °C which goes along with the weight loss step also determined by TGA. The evaporation of binding water is linked to changes in the confirmations of DNA-strands. The peak at around 120 °C already refers to melting of surfactant micelles and the peak at 148 °C corresponds to a glass transition. For usage in electronic devices films are not exposed to temperatures above 100 °C as insulating properties will change and confirmation changes will harm the electronic devices due to the sensitivity of interface properties.

3.4. Fullerene and Derivatives as Organic Semiconductor

OFET based on C_{60} has been reported in 1993 with field-effect electron mobility of 10^{-3} cm^2 $V^{-1}s^{-1}$ [22]. It was followed by a report from Bell Labs on the OFET with mobility of 0.3 cm^2 $V^{-1}s^{-1}$ in 1995 [23].

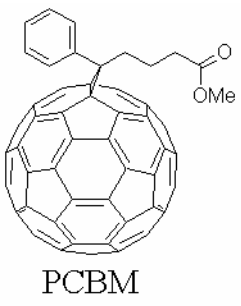

Figure 33 Soluble fullerene derivative: [6,6]-Phenyl-C_{61}-butric-acid methylester (PCBM)

Fullerene with side chains such as PCBM (Figure 33) have high mobility too (10^{-3} to 0.2 $cm^2 V^{-1}s^{-1}$) [24-25] and show generally n-type semiconductor properties. Recently it has been demonstrated for PCBM to have ambipolar transport, too [26-28]. Furthermore PCBM-based OFETs using polyvinylalcohol as gate dielectric offer hysteresis [1]. Singh *et al.* [22] demonstrated BiOFETs based on CTMA-DNA and pentacene performing at low operating voltage regime. The motivation in the present work is to fabricate n-type BiOFETs with all solution processed thin films. A soluble methanofullerene PCBM, a n-tpye organic semiconductor is used to successfully fabricate solution-processed bio-organic field effect transistors (BiOFETs) and memory elements. Electrical characterisation of the BiOFETs shows a promising low-voltage operating OFETs for use in organic electronics as a non-volatile memory element.

3.5. Device Architecture and Fabrication

All organic field effect transistors here are fabricated using bottom-gate/top contact structure borrowed from TFT-structure.

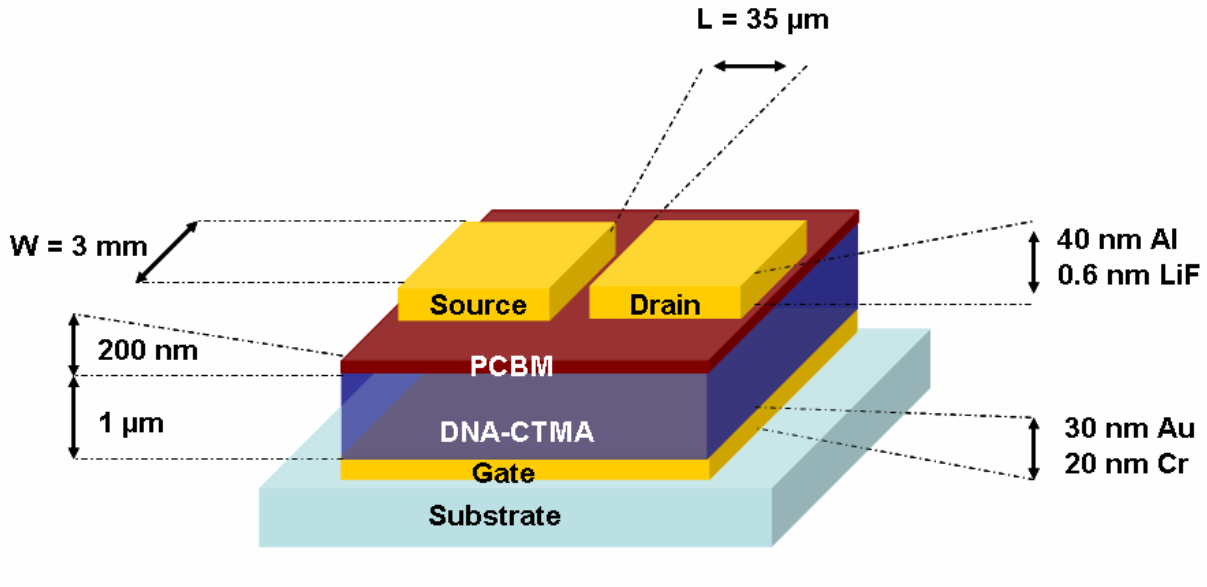

Figure 34 Top-contact/bottom-gate OFET structure including geometric device parameters

In Figure 34 the structure of a bio-organic field-effect transistor is presented. Dimensions of the channel lengh *L*, channel width *W* are provided as well as the z-cross section parameters including the 1 µm dielectric layer, a 200 nm PCBM and top electrodes. Apart from OFETs also 2-terminal devices are fabricated namely metal-insulator-metal devices (MIM) and metal-insulator-semiconductor-metal (MIS) devices depiced in Figure 35.

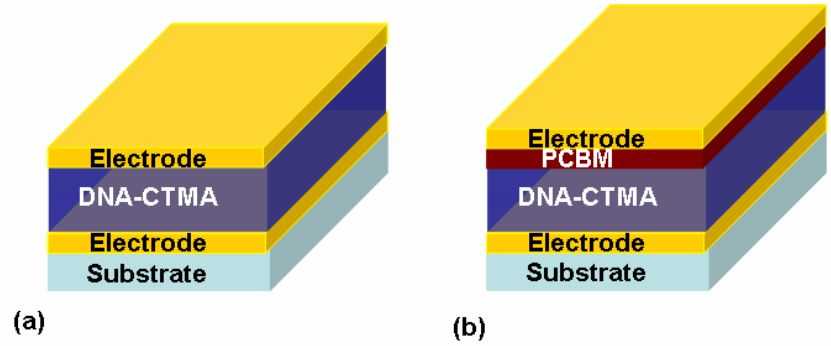

Figure 35 Two-electrode schematic "sandwich" device with both (*a*) a metal-insulator-metal (MIM) and (*b*) a metal-insulator-semiconductor-metal (MIS) device with embedded DNA-CTMA as dielectric layer.

The two-electrode devices use the same geometrical parameters as depicted in Figure 34 for the OFET structure. Except MIM top-electrodes on the PCBM film are LiF/Al which guarantees a good contact to the semiconductor. In case of MIM gold is used as both bottom and top electrode as work-function differences in non-symmetric device structure would be a disadvantage in measurements. For device fabrication square 15 mm x 15 mm borosilicate glas-plates are cleaned in ultrasonic bath of acetone and isopropanol followed by 2% alkalic cleaning concentrate Hellmanex dissolved in distilled water. After drying 20 nm Chromium and above 30 nm gold gate electrodes with an area of 15 mm x 3 mm are evaporated. Chromium as intermediate layer offers good adhesion properties to both glass and gold. From 300 kDa molecular weight DNA-CTMA dry power 10 weight % solutions in n-butanol are fabricated and stirred for a couple of hours in order to get a homogenous solution. After filtering with 0.2 µm filters DNA-CTMA films are spin-coated in ambient condition with a ration of 1500 rpm on the whole subtrate area. On one electrode-edge a small area of DNA-CTMA film is cut away in order to get a gate contact area of a couple of square milimeters. The thickness of the dielectric layer is probed by AFM measurements, the average values are around 1 µm. All the following steps from here on are done in inert Argon condition inside the glovebox. From PCBM powder 3 weight % solution in chlorbenzene is fabricated and stirred for a couple of hours and filtered. On top of the DNA-CTMA dielectric layer the PCBM is spin-coated again with a ratio of 1 500 rpm. For the source-drain top-contacts 40 nm LiF/Al is evaporated using a shadow mask with a 35 µm polycarbonate-fibre as channel cover. The area of the source-drain electrodes are 15 mm x 3 mm (respectively 5 mm). Separated metal-insulator-metal (MIM) devices and metal-insulator-semiconductor-metal (MIS) devices are fabricated either passing on the semiconductor layer and evaporationg a gold-contact on the DNA-CTMA layer (MIM) or evaporating a LiF/Al contact on top of

PCBM without a channel covering for the MIS-device. On top of a single substrate up to 3 parallel source-drain contacts and e.g. one top-electrode for MIS devices respectively can be evaporated. Finally in order to minimise contact problems small dots of silver are painted to the contact regions on the electrodes. The contact tips from the measurement equipment touches to the silver dots providing a good contact.

3.6. Device Probing Techniques

OFETs, MIS and MIM devices are probed with different techniques. Due to the interesting issue of bio-material as dielectric insulator, the emphasis is given on capacitance measurements as a function of an applied electric field and capacitance spectroscopy in order to detect the frequency dependence of the capacitance and dielectric constant respectively. Apart from capacitance *I-V* characteristics in all kind of devices are measured too, additionally in OFETs temperature dependence of transistor current I_{ds} is probed as well.

3.6.1. Metal-Insulator-Metall Devices

In order to proof the feasibility of thin DNA-CTMA films towards dielectric properties this metal-insulator-metal devices are suitable for capacitance measurements, quasi-static measurements and capacitance spectroscopy as well as *I-V* characteristics in order to investigate the polarisation behaviour of thin films, the influence of the scanning frequency in terms of changes in the capacitance and the remaining-conductivity as DNA-CTMA is considered to be a lossy dielectric.

Starting with *I-V* characteristics, the leakage current is matter of interest as losses in the insulating layer will influence the capacitance measurements. In terms of transistor the leakage current I_g also determines the current level minimum and sets the limit of significance in all current measurements done on devices using DNA-CTMA layers. *I-V* characteristics are done either in inert-gas atmosphere or in 10^{-6} mbar high vacuum condition. DNA-CTMA is hygroscopic which corresponds to the TGA-diagram in Figure 32 (*b*). Concerning conformation, geometric changes are negligible and films exposed to air will not be harmed but concerning electrical properties such as the conductivity and the capacitance an increase as a function of the ambient humidity is found.

Using the precision LCR-Meter 20Hz – 1 MHz the field-dependence of capacitance at a fixed AC-frequency is measured. These experiments are performed in inert condition in the glove box. For capacitance spectroscopy the sample is placed inside the cryostat with the base pressure of 10^{-6} mbar at constant temperature; the experiments are carried out in high vacuum condition with defined cable lengths and almost fully shielded BNC plug system using the high Performance Frequency Analyser (from 10 kHz to 0.1 mHz).

Quasi-static measurements are performed using the same cryostat-system as mentioned above. For this experiment slow positive and negative voltage ramps with a frequency of 1

mHz are applied to the sample and the current I_g measured with the 2 channel Source Monitor Unit as a function of time.

3.6.2. Metal-Insulator-Semiconductor Devices

In MIS structure especially the accumulation and depletion processes in the semiconductor as well as the mutual interface of the organic semiconductor and the DNA-CTMA dielectric are matters of interest. The origin of the remanent behaviours and the polarisation of the dielectric are investigated with capacitance measurements in high vacuum. Using the cryostat system with the high Performance Frequency Analyser, both the capacitance as a function of the field and the capacitance as a function of frequency (capacitance spectroscopy) are measured.

3.6.3. BiOFETs

A typical BiOFET output characteristics and transfer characteristics as well as retention curve measurements are performed using two-channel Source Monitor Unit. Besides, I_{gs} is measured to determine the minimum significance limit for I_{ds} in depletion regime. For investigation towards hysteresis, time parameter is introduced. Bistability or remancence of current states are measured at constant drain voltages V_d with cyclic pulses of gate voltages V_g between depletion-, ground- and accumulation-regime plotted as a function of time (switching). Corresponding single accumulation pulse measurements with a long retention time at ground gate potential are measured (retention time measurement). Retention curves are also measured at different temperatures T_s. For all current measurements the cryostat system introduced in 4.3.1 is used as it guarantees high reliability and reproducibility and as cables are shielded current measurements down to a range of 100 pA can be performed.

4. Results and Discussion

In terms of reproducibility results presented are based on several measurements and proofed several times in order to gain a reliable series of different experimental data.

4.1. Polarisation of DNA-CTMA

Before going to transistor the insulating bio-material is investigated towards electronic properties. DNA-CTMA films spin cast from n-butanol-solution are used as transistor gate insulator, so starting point is the polarisation of the bare DNA-CTMA film. Investigated by *I-V* measurements and quasi-static measurements, the main outputs are leakage currents and corresponding to this the stability of thin films at high electric fields as well as surface charge density from polarisation as a function of the voltage applied.

4.1.1 Leakage Effects and Electric Field Stability

The metal-insulator-metal device (MIM) is probed at high field in the range of MV cm^{-1}. Therefore devices with a 200 nm thin films are fabricated as mentioned in chapter 3.2.1., reducing the concentration of the DNA-CTMA in n-butanol to 1 %. The films are embedded with gold-electrodes and the current is measured as a function of the applied field. The results are presented below in Figure 36:

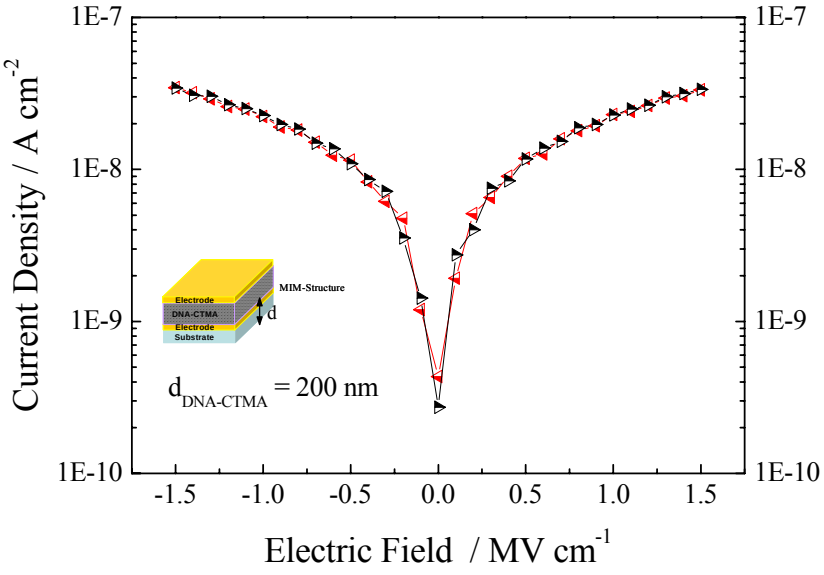

Figure 36 Scan of electric field versus the current density shows stability of DNA-CTMA.

From the experimental data one can assume high stability of the dielectric upon applied high electric field. The upper regions of a couple of MV cm^{-1} are not even reached in terms of BiOFET – probing. Average field strengths are approximately in the region of 150 kV cm^{-1} or slightly higher also depending on the device geometry. This measurement also sets the minimum limit of significance in terms of transistor current experiments and represents the starting point of the whole investigation towards electronic properties of DNA-CTMA films.

4.1.2. Quasi-static Experiment

In Figure 15 (chapter 2.4) measurement of the surface charge density in metal-insulator-metal capacitor device is presented using a Saywer-Tower circuit measurement setup. This results show hysteresis loops of polyvinylidenefluoride-trifluorethylene copolymer, which offers intrinsic hysteresis effects due to non-centro-symmetrical crystalline regions in the polymer-film. Already known as lossy dielectric matter of interest is to probe, if DNA-CTMA shows non-linear charge polarisation effects, as demonstrated in the case of the fluoric – copolymer from Figure 15. As Sawyer-Tower setup is not available DNA-CTMA films are probed using quasi-static measurement.

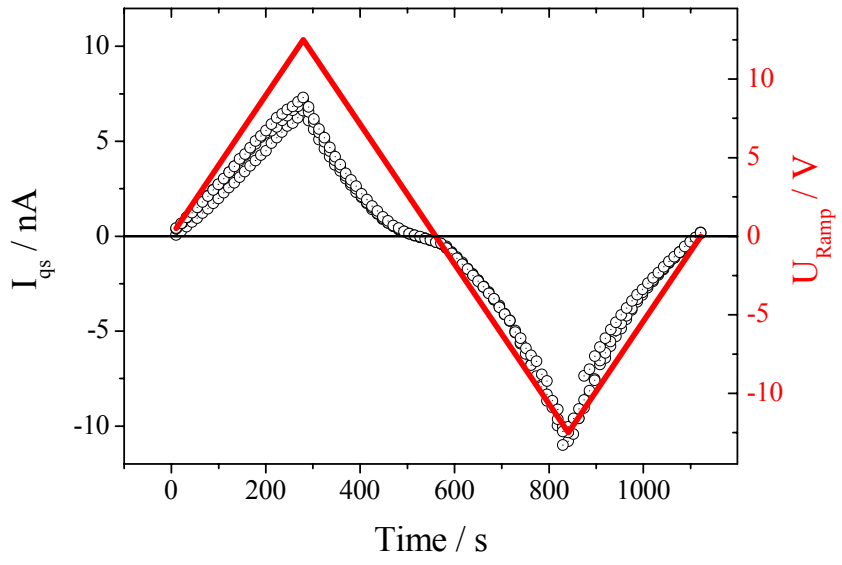

Figure 37 Quasi-static measurement: As a function of an applied slow cyclic voltage ramp the current is measured versus the time.

From the shape of the current-characteristics a slight non-symmetric behaviour is detected. This refers to device fabrication, because the insulator is spin-cast onto the bottom-electrode whereas the top-electrode is deposited by evaporation. Diffusion of gold into the insulator

cause non-symmetric effects, another reason can be temperature-increase during the measurement. Ideally the current flow shall represent the remaining part when a capacitor is acting as resistor in an AC-circle at very low frequency (quasi-static AC). The quasi-static current I_{qs} is proportional to the number of surface charges Q_s on the polarised film at a certain field.

$$D_s = \frac{Q_s}{A_{Electrode}} = \frac{1}{A_{Electrode}} \int_{t=0}^{t} I_{qs} \cdot dt \qquad (16)$$

Derived from equation (16) the surface charge density D_s is calculated and plotted versus the applied gate voltage V_g.

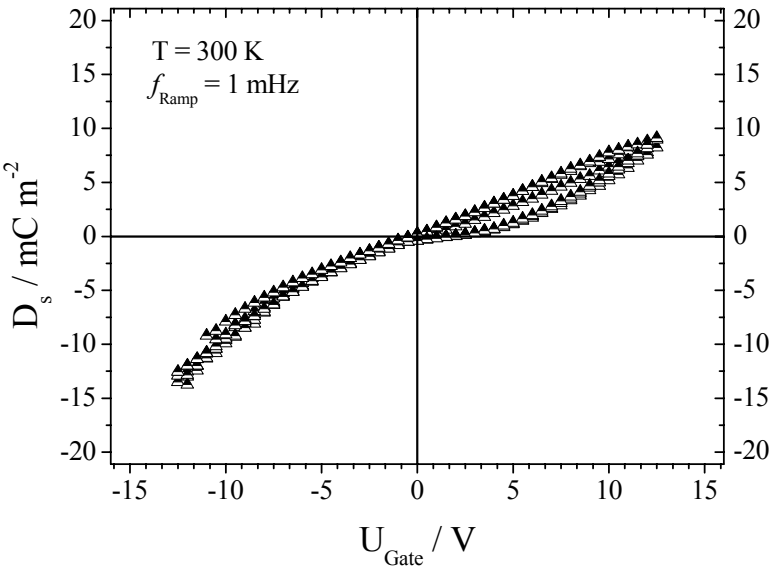

Figure 38 Quasi-static measurement: Linear charge polarisation in low-frequency region.

Comparing the values of the surface charge density with those of Figure 15, the difference is one order of magnitude when the ratio of the applied field to the amount of surface charges is considered. Going back to the main issue, DNA-CTMA does not have non-linear charge polarisation and is considered as linear lossy dielectric. This conclusion is borne by the fact that the curves in Figure 38 pass the point of origin. It is to be noted here that DNA-CTMA have been shown no-linear optial (NLO) effect [17].

4.2. Low Operating Voltage BiOFETs

From the polarisation measurement interesting performance can be expected from BiOFETs. One issue is to present a transistor operating at voltages below 10 V, the other one is the

understanding of the channel forming process and linked to that the construction of memory-elements. The output characteristics of the BiOFET presented in Figure 39 at different gate voltages show saturation above 20 V. The scan rate is set at 250 mV s^{-1} Interesting issue is that the transistor already shows currents in the range of µA at gate voltages below 10 V.

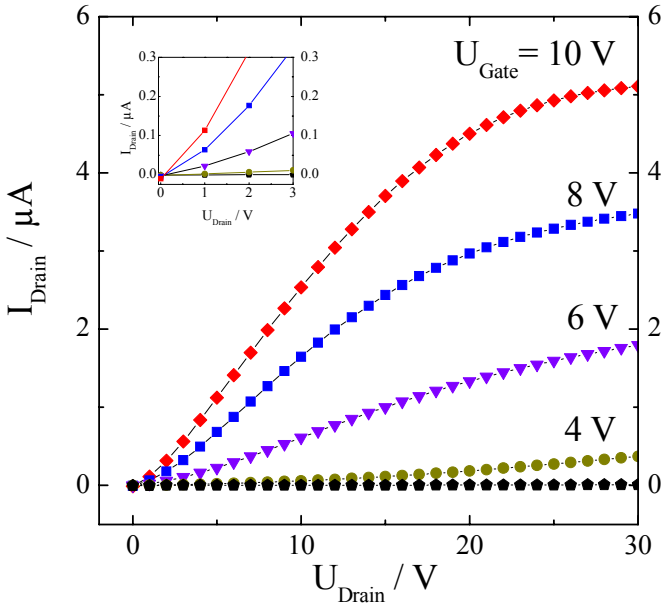

Figure 39 Output characteristics of solution-processed low voltage operating BiOFET with scanning voltage steps of 250 mV s^{-1}. Inset: Zoom of low V_d region which shows non-linear increase from overlapping contact resistance.

Drain current does not saturate at $V_d = V_g$ which indicates a severe contact resistance and hence a voltage drop at the charge injecting electrode. This voltage drop is proposed to cause the shift of the saturated I_{ds} at higher V_d [29].

4.2.1. Hysteresis in Transfer Characteristics

Figure 40 presents the transfer characteristics which represents the transistor current I_{ds} plotted as a function of the gate voltage at constant V_d. The scan is repeated three times with different drain voltages, the scan rate is set at 12.4 mV s^{-1}.

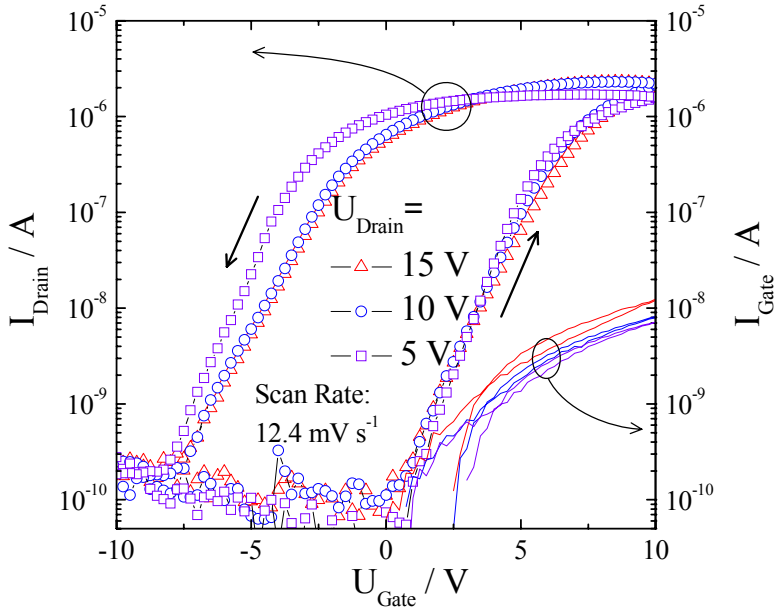

Figure 40 Transfer characteristics of BiOFET: All measurement are performed with steps of 12.4 mV s^{-1}. Note: Gate current characteristics of the BiOFET is also plotted and corresponds to the right hand scale of the graph.

At low scan rate the whole extent of hysteresis is demonstrated. Following the forward curve the transistor turns on near 0 V and current increases up to four orders of magnitude showing a saturation at V_g = 10 V. These results indicate a drain current independent of drain voltage in the saturation regime satisfying equation (4). The scale on the right side represents the leakage current I_g from the gate. It is considered to be negligible as it represents less than 1 % of the transistor current I_{ds}. Seen in the reverse scan the transistor current remains constantly high when the gate voltage is reduced unless a depletion voltage is applied from the gate. Current in the reverse direction decreases with the identical slope as in the forward direction. When the scans are focused on V_g = 0 V (grounded), two current levels – "on" and "off" – are seen with a difference of 4 orders of magnitude. From the transfer characteristics it is not answered how stable the current will be in this meta-stable "on"-state.

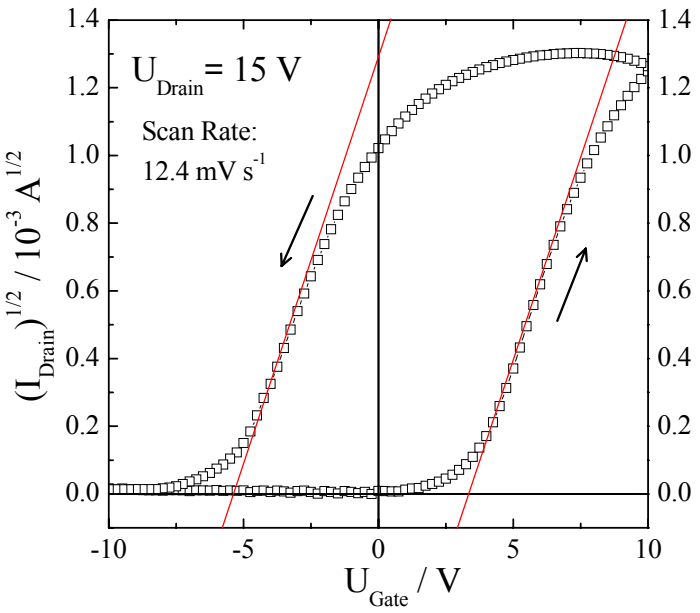

Figure 41 Square root of I_{ds} versus the gate voltage at saturated V_d regime including linear dependency shown in forward and back scan. At the intersection with the x-axis (red line) the threshold-voltage can be estimated.

Since BiOFET transfer characteristics shows a large threshold voltage shift of around 10 V it is rather difficult to estimate accurate charge carrier mobility μ of the organic transistor. Depicted in the square root plot the real onset voltage shift is seen. As hysteresis are strongly dependent on the scan rate, the voltage shift is also expected to depend on the scan rate. It also clearly observed in the reverse direction of the gate voltage sweep, the current even increases further (see Figure 41). Interestingly this increase is attributed exactly to the additional quasi-permanently polarisation. Calculations can be performed easier when measuring the current at constant fields from both the gate V_g and the drain V_d.

4.2.2. Retention Behaviour

To study the transient response of on-state and off-state of an organic FET memory element one can measure retention curve. The more stable is the current is the better for using memory element. This measurement is performed with a pulse of gate voltage applied to the OFET memory element as shown in Figure 42.

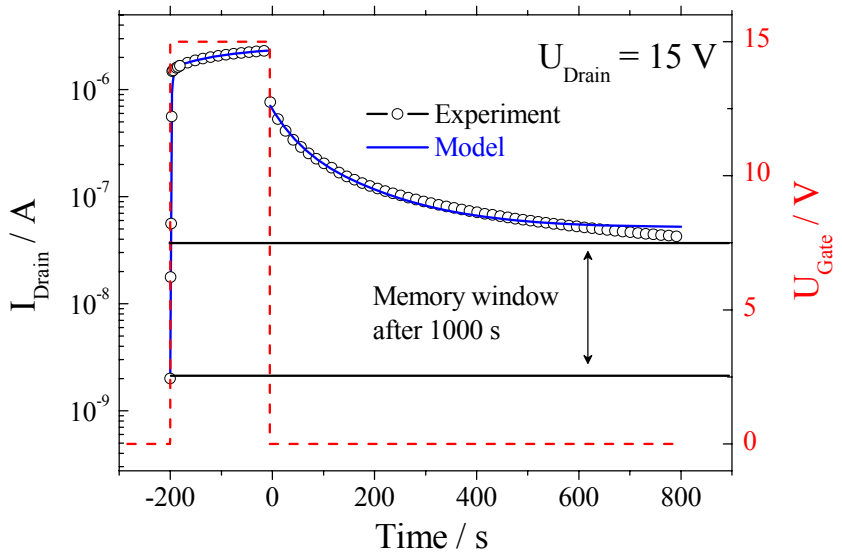

Figure 42 Retention curve (symbols) at V_d = 15 V indicating a fast rise of the drain current followed by slow saturation and very slow decay of the drain current when gate voltage is reduced to 0 indicating a long retention time. A theoretical fit is also presented (solid line) using equation 17 with the parameters given in Tabel 2.

This fit using a double exponential equation (17) describes the current-increase as well as the current decay before, during and after the gate voltage pulse.

$$I_{ds}(t) = A_1 \cdot e^{-\frac{t}{\tau_1}} + A_2 \cdot e^{-\frac{t}{\tau_2}} + I_0 \qquad (17)$$

It is a forced fit. Parameters are given in table 2. The first time constant represents the fast channel forming due to polarisation of the dielectric, seen in an immediate increase of the current. The second time constant refers to the continuing increase of current flow at constant accumulation field. This time constant corresponds to the slow polarisation is two orders of magnitudes slower and can be attributed to the movement of slow charges in the dielectric with an electric field leading to further polarisation at the interface and consequently further injection of charge carriers. The memory window after 800 seconds retention time after the accumulation pulse is illustrated. From -200 to 0 seconds the transistor is pulsed from grounded potential to accumulation regime and this current increase process is modelled, also depicted in the graph.

Equation (17) describes the current increase as a function of time. The constants A_1, A_2 and I_0 summarise the device geometry, mobility, geometric capacitance etc. Important outputs are the two time constants τ_1 and τ_2: From the experimental data for $\tau_{inc,1}$ values of 3.2 s, for $\tau_{inc,2}$ 140 s are calculated. From 0 to 800 seconds the accumulation pulse is removed (de-pulsing)

and the current decreases following the same model-fit in equation (17). It is valid for the de-pulsing process, again a fast decay is followed by a slow one represented in two time constants using equation (17) in order to describe the curve. The fast constant $\tau_{dec,1}$ is in the range as for increase set at 34.5 s, the second constant $\tau_{dec,2}$ is calculated at 137 s. Generally separating the channel forming and channel de-forming respectively in a fast and a slow process makes sense and approaches close to the theory of charge movement and charge trapping in the interface of the organic semiconductor and the dielectric. The slow processes explain fairly well the bistability–hysteresis region in these bio-organic field effect transistors.

Table 2 Parameters of retention-curve fit presented in Figure 42.

Process	A_1 [µA]	A_2 [µA]	I_0 [µA]	τ_1 [s]	τ_2 [s]
Increase	-1.00	-1.89	2.57	3.20	140
Decrease	1.19	110	0.0516	34.5	137

The retention measurement presented above is repeated, this time the amplitude of the gate voltage pulse is modulated. The current levels are different depending on the accumulation amplitude-potential, but the shape of the increase as well as the current decay after the de-pulsing back to ground potential remains the same, seen in Figure 43.

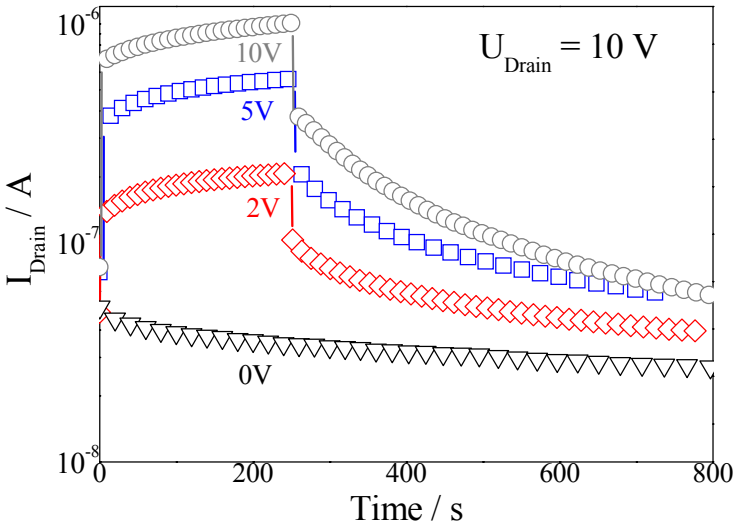

Figure 43 Transient single pulse response-characteristics of BiOFETs indicating a long retention time at four different accumulation potentials.

The drain voltage is set a 10 V. On the left side the gate potential starts from ground state (V_g = 0) followed by a 250 second gate pulse with 4 different amplitudes (V_g = 10, 5, 2 and 0 V). While at ground potential V_g = 0 one sees a straight line, the current increases immediately after a pulse and continues increasing at constant accumulation potential. When it is removed to ground state again, the decay observed is fast at the beginning and saturates after some time.

4.2.3. Temperature Dependence

Temperature dependence transient response of BiOFETs gives a insightful underline phenomena of charge movement in the bulk of the insulator and on the surface as origin of the hysteresis.

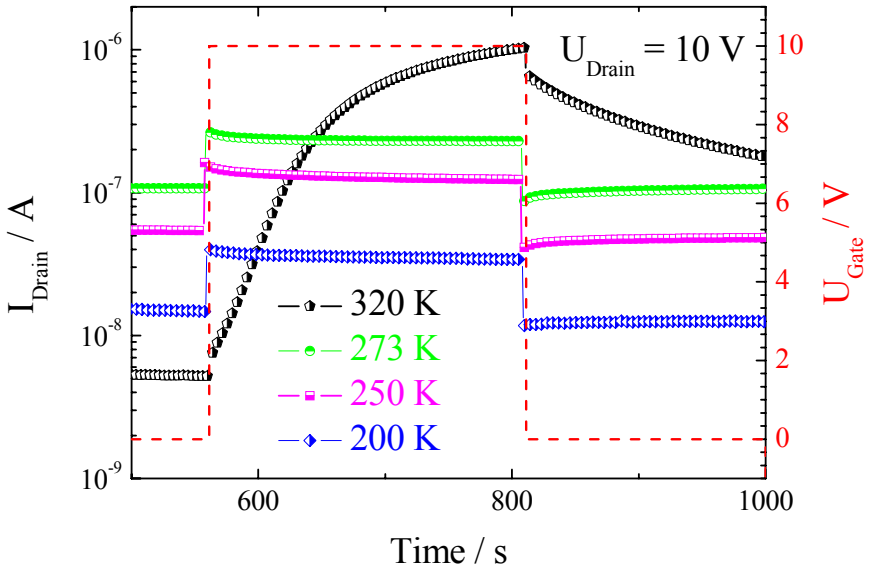

Figure 44 Temperature dependent transient decay charactersics of BiOFET when a pulse of gate voltage with pulse height shown in right hand scale.

Figure 44 shows temperature dependent remanent behaviour of the BiOFETs in the temperature range between 320 K – 200 K. At 273 K the current already follows precisely the shape of the voltage pulse without any further charging.

The metatable “on” state vanishes, the current drops back to the off-state when the pulse is switched off. In this case charge carriers in the bulk-insulator are immobilised and do not cause a quasi-permanent polarisation of the dielectric layer. Here two competing factors contribute to the magnitude of the drain current: (*i*) Temperature dependent mobility $\mu(T)$ and (*ii*) Temperature dependent mobility of charge carriers in the bulky of the dielectrics. Time

constants for increase in pulsing as well as decrease are not comparable, for two competing factors will change the current level.

4.2.4. Switching Experiment (Memory Element)

With the fact that transfer characteristics of the BiOFET (Figure 40) and long retention time (Figure 42) here a memory element is demonstrated (see Figure 45). Starting from the left side one takes cross-sections at depletion regime (V_g = -10 V), at bistable grounded regime (V_g = 0 V) and at accumulation regime (V_g = 10 V). Setting the drain voltage V_d constant at 15 V, the transistor is pulsed with these three gate voltage regions. The pulsing time is set to 50 seconds and the current measured as a function of time.

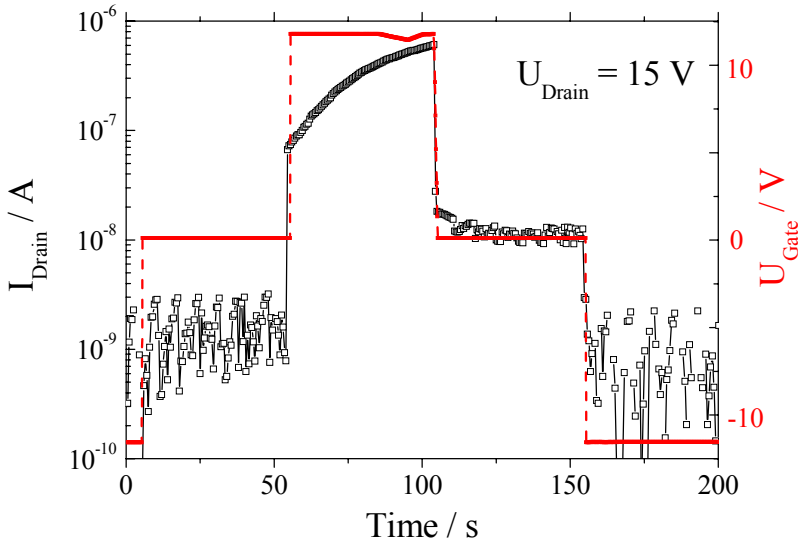

Figure 45 Transient decay characteristics of BiOFET with different gate bias condition as a memory element wih an applied gate voltage pulse showing memory "off", "write", "on" and "erase". Height of gate voltage pulse is shown in the right hand scale..

The result is presented in Figure 45: Red line is the gate voltage (square wave pulse, dashed line) the symbols are the drain current. It starts from the left side with depletion followed by the ground gate potential. At the accumulation pulse the current increases immediately two orders of magnitude. At constant accumulation field the current continues to increase describing a logarithmic shape which shall lead to saturation. When the ground voltage pulse is applied again, the current decreases – not to the depletion level from backwards but to a metastable state between accumulation and depletion. This state is at least one order of magnitude higher than the depletion state, in which the current drops back after the depletion

pulse. This circle can be repeated many times. In terms of memory element as presented in chapter 2.5 (Figure 19) the four states are called “write” at accumulation, “on” at the intermediate metastable state, “erase” at the depletion pulse and “off” when the gate is grounded and a new circle will start once more. The memory circle can be repeated many times.

4.3. Capacitance Measurements

In BiOFETs the output always concerns the transistor current I_{ds}. Additional information of the transistor working principle and for advanced understanding of the interfacial phenomena can be observed using capacitance measurements.

4.3.1. Capacitance Spectroscopy

From both devices, MIM and MIS capacitance is measured as a function of the AC frequency. The AC amplitude is set at ± 0.5 V. Injection processes in the MIS devices can be neglected at this AC voltage amplitude. The output is the geometric capacitance C_p and the loss factor tan(δ).

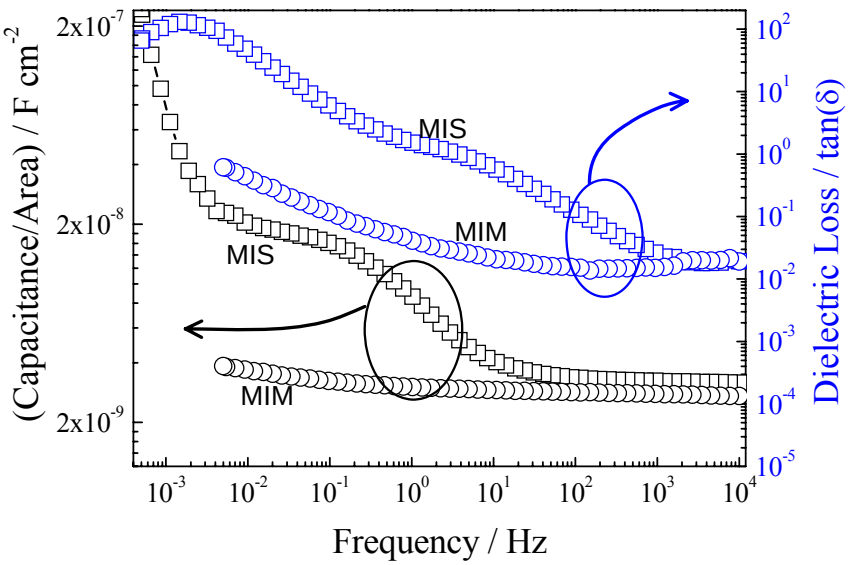

Figure 46 Room-temperature capacitance-frequency of both MIM and MIS structure devices (with applied a.c. voltage of 0.5 V). On the right hand side dielectric loss is also shown.

In the diagram above, in case of both, MIM and MIS device, the capacitance is plotted as function of the frequency *f*. The dielectric properties of the DNA-CTMA layer start to change

when scanning downwards to low frequencies. Starting with the MIM device, an increase in capacitance is observed which relates to charge carriers in the bulk of the insulator and gives a response only at low frequencies and low field changes respectively. In fact the DNA-CTMA material though to good insulating properties is suspicious to have ionic species inside, which cause this quasi-permanent polarisation including trapping of charges at the interface to the semiconductor. Ions respond due to their low mobility in the matrix only to low field changes in the range of 55 mV s^{-1}, and as plotted in Figure 44, they are immobilised when cooling down to 0 °C and below. The overall capacitance increase corresponds to the dielectric loss characteristics, when the resistance of the dielectric at low frequency decreases.

When looking at the MIS – curve the capacitance increases by almost one order of magnitude at lower frequency, building a second plateau. At frequencies below 10 mHz the capacitance rises once again.

The frequency – dependent capacitance changes arise because of presence of two different capacitors. The dielectric layer is represented by the DNA-CTMA which dominates at high frequency range. The semiconductor layer is represented by the fullerene-derivative, which dominates at frequency ranges below 10 Hz. The layer-by-layer addition of capacitors should follow the Maxwell-Wagner equation for lossy dielectric capacitors (chapter 2.5). As seen in Figure 46 for the MIS double-layer device the plateau-building is not sharp as suggested in the theoretical approach. We assign these effects to interactions between the semiconductor and the dielectric at the interface. Besides an additional capacitance increase in the sub-mHz regime is observed. Setup limitations do not allow capacitance scans to even lower frequencies. Electrode polarisation effects between the top-Aluminium-electrode and the PCBM interface are suggested to cause the additional capacitance increase.

4.3.2. Capacitance vs. Electric Field and Scan Rate

Studies on MIM devices, when applying a field across the device have been presented in the quasi-static experiment. Expected due to ionic movement measurement in mHz regime the DNA-CTMA shows linear lossy properties in terms of polarisation. In case of MIS, first of all the remanence behaviour is a matter of interest, so the double layer device is scanned with different field-rates and the capacitance measured as a function of the field. Second by applying a sufficient high field to the device, injection processes are observed.

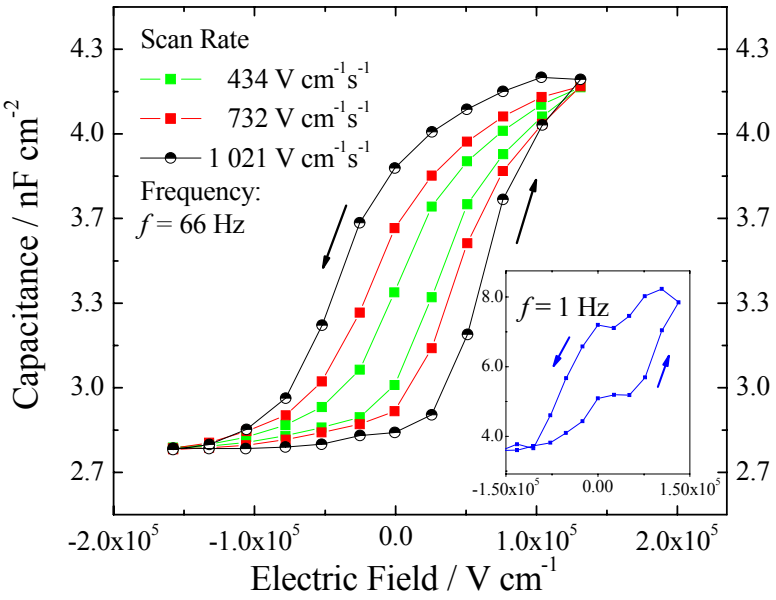

Figure 47 Quasi-static capacitance-electric field curves fr the MIS structures (at 66 Hz) at different scan rate as indicated. Inset shows quasi-static capacitance-eletric field curve of MIS at 1 Hz with scan rate of 1 021 V cm-1 s-1. Larger hysteresis with slower scan rates are found.

In Figure 47 the results are presented, three different curves at different scan-rates. It applies to the lower the scan rate the greater the extend of the hysteresis. It goes along with the quasi-static polarisation of the dielectric, these charge diffusion in the bulk of DNA-CTMA and the interface. Charges move to the interface and they are trapped there, only a field in the opposite direction will remove these carriers. For sure, at slower scan rates the effect will be more distinctive. The AC frequency in the measurement circle is set at 66 Hz, which is in constant dielectric regime, when reminding the capacitance spectroscopy. Choosing an odd number, interferences with the 50 Hz AC surrounding are avoided. In the inset, field dependence of the capacitance is measured at 1 Hz. In this frequency regime, the semiconductor plateau is reached, which corresponds in the increase of capacitance when comparing it with the 66 Hz experiments.

In order to explain the increase of the capacitance we just look at the injection process monitored with the capacitance at 66 Hz. It is compared to a Schottky diode of an organic semiconductor [30], when a doped semiconductor layer forms next to the interface of the dielectric DNA-CTMA layer. In Figure 48 the inverse square capacitance of the results from Figure 47 (at two scan rates) is demonstrated as a function of the applied field. Hence, carrier

injection to the n-type semiconductor is seen and this is related to the charge-carrier density N_A due to interfacial doping in the MIS diode:

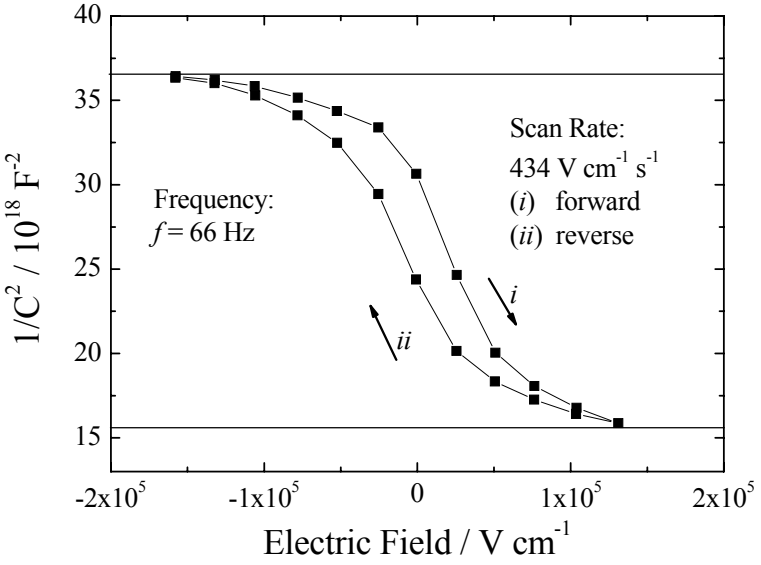

Figure 48 Inverse square capacitance as a function of applied field of the MIS diode for a fast scan (compare Figure 47).

Charge carrier density N_A in the semiconductor is expected to reach high values, for experiments in BiOFETs show reasonable high transistor currents (see Figure 40). Matter of interest is to calculate N_A. Generally the capacitance increase for a doped organic semiconductor should follow linearly the Schottky-barrier equation.

$$\frac{1}{C^2} = \frac{2 \cdot (V_{Th} - V)}{A^2 \cdot q \cdot \varepsilon_0 \varepsilon_R \cdot N_A} \qquad (18)$$

C	Capacitance of MIS diode	A	Area of the capacitor plate
ε_0	Permittivity of free space	N_A	Charge carrier density
ε_R	Dielectric constant of semiconductor (PCBM)	q	Charge of carriers

Even if the shift in the electric field due to hysteresis (compare: scans in forward and reverse direction) might allow a calculation of an average threshold voltage V_{Th}, the calculation of the charge carrier density is unreasonable. First of all the influence of the AC-frequency is to be discussed, as the injection process from the source has a certain time-limitation. Further experiments at higher frequencies are needed, where the capacitance increase remains constant. Secondly the capacitance-increase saturates at higher fields. Therefore injection process is stopped at a certain region.

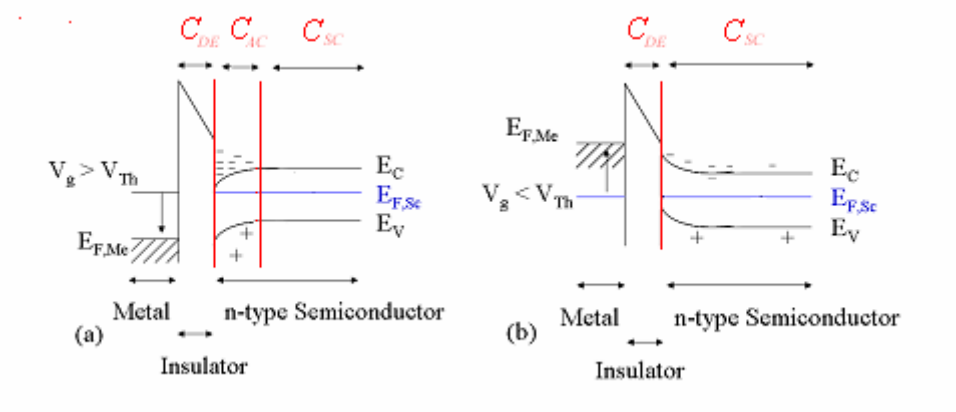

Figure 49 Schematic view of dielectric polarisation with (*a*) and without (*b*) injection of charge carriers to a n-type semiconductor. In (*a*) the total capacitance *C* of the device is changed due to injection of carriers. Next to the interface an additional capacitor C_{Ac} arises (interfacial doping of the semiconductor).

Figure 49 shows schematically the injection process in a MIS device. C_{DE} is the capacitance of the DNA-CTMA layer and C_{SC} is the capacitance of PCBM. C_{Ac} refers to the narrow heavily interfacial-doped PCBM-semiconductor layer, which arises as a function of the field in accumulation voltage regime. As depicted in Figure 49 (*a*) three serial capacitors arise. It goes along with a change of the total capacitance and consequently we obtain an increase in the capacitance (Figure 47).

4.4. Discussion

We assign the hysteresis to charge movement in the bulk of the dielectric to the interface, trapping and de-trapping processes with restricted mobile charge-species. This is supported by the measurements, e.g. seen in capacitance spectroscopy. In case of MIM device at frequencies below 100 mHz charge movement in the dielectric leads to a rise in the capacitance. Presence of charges or ions in the dielectric is detected when scanning the capacitance at low AC frequencies. Different case concerns the MIS devices, where plateau building is observed, which is assigned to the semiconductor layer. Only at the first view, because with a simple model adding layer by layer and fit the device with a sum of impedances only roughly describes the MIS device.

The saturated drain currents are found to be bistable at gate voltages V_g around 0 V. As shown in the transient characteristics (Figure 42) drain current is measured as a function of a pulse gate voltage. Once saturated, drain current is obtained with an applied gate voltage saturated drain current remains high for more than 800 seconds, even after gate voltage V_g is reduced to 0 V, indicating a long, charge carrier retention time. A theoretical fit to the experimental data using a double-exponentially equation yields two components, namely a fast charging and a slow charging time constant of 3.2 s and 140 s for accumulation. Similarly for decay of saturated drain current a fast decay and a slow decay time constant of 35 s and 137 s respectively are extracted.

A number of devices were characterized as a function of temperature T_s for hysteresis and the details of a representative device is presented here. As these devices possesses a large channel resistance R_i, it is unreasonable to report the saturated mobility, μ or saturation conductance, g_m as R_i is generally known be to strong temperature dependent. However to study the trapping/detrapping as a function of temperature we have measured the transient decay of $I_{ds,sat}$ at various T_s. Figure 44 shows the transient curve of $I_{ds,sat}$ as a function of applied single V_g pulse for different T_s. At higher T_s, $I_{ds,sat}$ rises and decay significantly slowly compared at lower T_s. At lower T_s which attributes to charge species which are responsible for the “slow polarisation” is no longer mobile.

5. Conclusion

From the results presented in the thesis two messages are important: At first DNA-CTMA is a good dielectric insulator for use in organic electronics – measured devices show remarkable performances in terms of low voltage functionality. Secondly remanent characteristics are applicable for non-volatile BiOFET memory elements. Consequently we try to understand the relevant processes going on in the DNA-CTMA dielectric and find out experimentally the origin of hysteresis qualitatively. It seems to be interplay of mobile charges in the bulk and the surface, which can be transported by a field. When the BiOFET is filleted into its particular compounds e.g. presented in quasi-static experiments, these remanent features arise from the interface of the DNA-CTMA and the semiconductor. Intrinsic remanent characteristics are not observed in bare DNA-CTMA films or bare PCBM diodes.

The BiOFET output characteristics are separated into two effects, a fast and a slow one: Slow effects are detected at low scan rates and DC respectively. Applying a constant field from the gate across the device, trapping/de-trapping mechanisms of charges cause a quasi-permanent polarisation of the dielectric-semiconductor interface. It indicates mobile charges in the DNA-CTMA – semicondcutor interface layer. Interestingly these mobile charges can be immobilised by annealing and as a consequence hysteresis effects minimised at temperatures below 273 K. Immobilised charges in the bulk do not affect the semiconductor, only when charges are mobile quasi-permanent polarisation takes place. The injection process in the semiconductor is driven by the enhanced polarisability of the dielectric.

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7. List of Figures

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Contribuions to conferences

7/2006	“*Bio-organic Field-Effect Transistor Memory Elements*”
	P. Stadler, T. B. Singh, R. Schwödiauer S. Bauer and N. S. Sariciftci
	Talk at the ICSM 2006 Dublin (Ireland)